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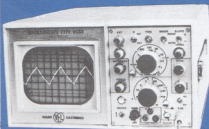


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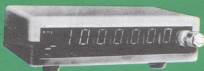
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## HIGH LEVEL WIDEBAND RF PREAMPLIFIER

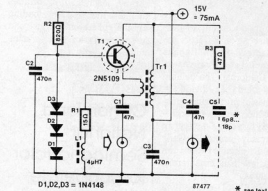
A linear RF amplifier can be made in two ways: (1) with the aid of a linear active element, or (2) with a non-linear element operating with negative feedback. This circuit is of the second kind, using an RF power transistor as the active element. Feedback is also required to ensure correct termination (50  $\Omega$ ) of the aerial, since bipolar transistors normally exhibit a low input impedance. Also, the noise figure is not increased because virtually no signal is lost.

The common-base amplifier is based on a UHF class A power transistor Type 2N5109 from Motorola. The feedback circuit

is formed by RF transformer Tr<sub>1</sub>. The input and output impedance of the preamplifier is 50  $\Omega$  for optimum performance. Network Rs-Cs may have to be added to preclude oscillation outside the pass-band, which ranges from about 100 kHz to 50 MHz. The gain is approximately 9.5 dB, the noise figure is between 2 and 3 dB, and the third-order output intercept point is at least 50 dBm.

The input/output transformer is wound on a Type FT37-75 ferrite core from Micrometals. The input winding is 1 turn, the output winding 5 turns with a tap at 3 turns.

5



\* see text

# 2

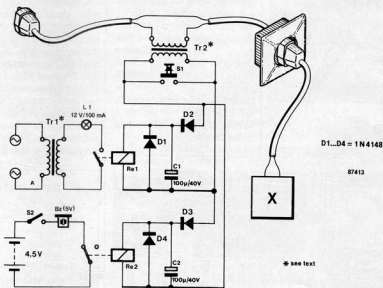
# MAINS FAILURE ALARM

by A Treps

This circuit was originally developed to detect and signal interruptions of the mains supply to artificial respiration systems. The signalling is done in two ways: a buzzer is sounded, and a small lamp is quenched.

The supply current to the monitored equipment induces a variable flux in a small transformer that serves to keep the relays actuated, so that  $L_{a1}$  lights and  $Bz$  is off when the mains voltage is available. When a mains failure occurs, apparatus  $X$  no longer draws current, so that both  $Re_1$  and  $Re_2$  are de-actuated, resulting in the lamp being turned off, and the battery-operated buzzer being activated.

Transformer Tr<sub>2</sub> is a modified 3 VA mains type which functions as a current transducer: the original primary winding functions in this application as the secondary, while the original secondary winding is replaced by about 7 turns of 20SWG (Ø 1 mm) enamelled copper wire. Every precaution should be taken to ensure that



\* see text

the new winding is capable of safely handling the current demand of X. Thanks to the so created high turns ratio in the transformer, a relatively small current suffices to keep the relays actuated and the smoothing capacitors  $C_1$ - $C_2$

charged. Push-button  $S_1$  makes it possible to test the alarm by simulating the absence of induced current.  $Tr_1$  can be a small bell type, or one salvaged from a mains adapter for a pocket calculator. Switch  $S_2$ , finally, is used to turn off the

buzzer when apparatus X is disconnected or switched off.

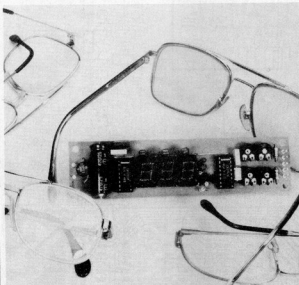
R



This V/I display module is eminently suitable for building into an existing DC power supply, where it gives a precise indication of the set voltage or the current consumption of the load.

The circuit diagram appears in Fig. 1. The 3-digit readout is based on A/D converter Type CA3162 and BCD-to-7 segment decoder Type CA3161, both from RCA. The common anode connections of LED displays LD<sub>1</sub>-LD<sub>3</sub> are successively connected to the positive supply line via T<sub>1</sub>-T<sub>3</sub>.

Provision has been made to select the correct position of the decimal point. In the voltage range, the decimal point lights on LD<sub>1</sub>, and the resolution is therefore 100 mV. Two current ranges are possible: 0-9.99 A (link a) or 0-0.999 (999) A (link b). The current sensing resistor is therefore either 0R1 or 1R0—see Fig. 2. It is important that R<sub>s</sub> does not affect the output voltage. It must, therefore, be fitted ahead of the voltage divider that con-



trols the output voltage. DPDT switch S<sub>1</sub> selects between voltage and current readings. When voltage measurement is selected, P<sub>1</sub>-R<sub>1</sub> attenuates the input voltage by a factor 100. Also, point D is pulled low so

that the decimal point on the LS display, and the "V" LED, are illuminated. When current measurement is selected, the drop across the sensing resistor is applied direct to the HI-LO inputs of DAC IC<sub>1</sub>. The sensing resistor has such a low value as

to render the voltage divider

ineffective. There are four adjustment points in the module:

P<sub>1</sub>: current range nulling;

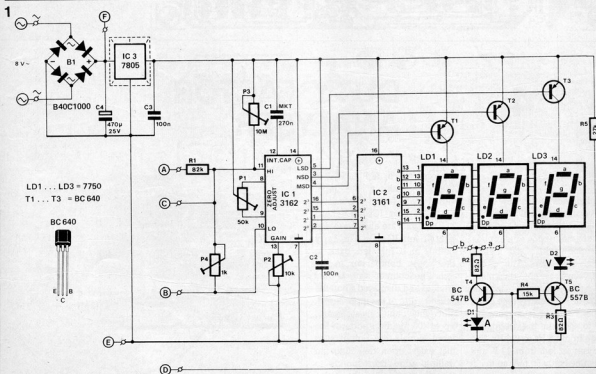
P<sub>2</sub>: full-scale current calibration;

P<sub>3</sub>: voltage range nulling;

P<sub>4</sub>: full-scale voltage calibration.

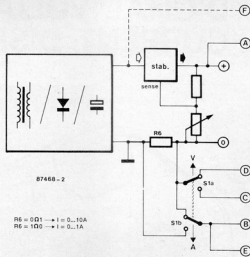
These points should be adjusted in the above order. Two presets, P<sub>1</sub> and P<sub>3</sub>, are required to ensure correct nulling of the module. P<sub>1</sub> compensates for the quiescent current consumption of the regulator circuit in the supply. The resulting small negative deviation in the voltage range is compensated by P<sub>3</sub>.

The V/I display module is conveniently fed from the unregulated voltage available in the supply (max. 35 V)—see points E and F in Fig. 2; bridge rectifier B<sub>1</sub> may then be omitted. The minimum input voltage for IC<sub>1</sub> is 8 V, and this regulator should be fitted with a heat-sink if the input voltage is greater than 12 V. It is, of course, also possible to power the module from a separate 8 V; 200 mA mains transformer.



The unit can be constructed as a double to obtain simultaneous V and I readings. It should be noted, however, that the current sensing resistor is short-circuited via the ground connections when both modules are fed from the same supply. There are two ways to overcome this problem. One is to feed the V unit from a separate supply, and the I unit from the "host" supply. The other is more elegant and entails hard wiring points E to the left side of the current sensing resistor. Note, however, that the highest V indication then becomes 20.0 V ( $R_s$  drops 1 V max.), since the voltage at pin 11 may not exceed 1.2 V. Higher voltages can be displayed by selecting the lower current resolution,

2



i.e.,  $R_s$  becomes 0R1. Example:  $R_s$  drops 0.5 V at a current consumption of 5 A, so that  $1.2 - 0.5 = 0.7$  V remains for the voltage indication, whose maximum reading is then  $100 \times 0.7 = 70$  V. Again, these complications only arise when two of these modules are used in a single supply.

TW

#### Parts list

Resistors ( $\pm 5\%$ ):

- $R_1 = 82K$
- $R_2, R_3 = 82R$
- $R_4 = 15K$
- $R_5 = 27K$
- $R_6 = 0R1$  or  $1R0^*$
- $P_1 = 50K$  preset
- $P_2 = 10K$  preset
- $P_3 = 10M$  preset
- $P_4 = 1K0$  preset

Capacitors:

- $C_1 = 270n$
- $C_2, C_3 = 100n$
- $C_4 = 470 \mu, 25 V$

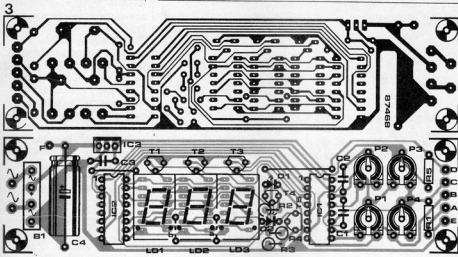
Semiconductors:

- $D_1, D_2 = LED$  red
- $B_1 = BC40C1000$
- $LD_1, LD_2, LD_3 = 7750$
- $T_1 \dots T_3$  incl. =  $8C640$
- $T_4 = BC547B$
- $T_5 = BC557B$
- $IC_1 = CA3162$
- $IC_2 = CA3161$
- $IC_3 = 7805$

Miscellaneous:

- $S_1 =$  miniature DPDT switch.
- PCB Type 87468 (see Readers Services).

\* See text.



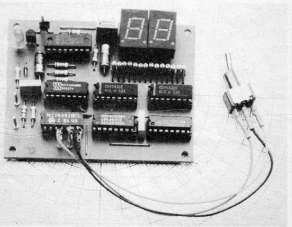
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## DUTY FACTOR ANALYSER

by R. Behrens

Applications of this duty factor meter include adjusting and setting up ignition systems, switch mode power supplies, PD modulators, and sensor signal converters. The circuit itself requires no adjustment, and has a duty factor resolution of 1%, or 1° in terms of the dwell angle. The duty factor range is 1% to 99% in the frequency range from 1.5 Hz to 10 kHz. The analyser is fed from 12 V and consumes only 50 mA, so that it can be readily used in a car. The measuring principle is

straightforward. A PLL,  $IC_5$ , is used to multiply the input signal by a factor 100 and to clock counter  $IC_6-IC_7$ , whose BCD outputs are applied to display drivers  $IC_2-IC_3$ . The carry output of  $IC_7$  is fed back to the phase comparator in the PLL. The counter state is only latched and displayed upon the falling edge of the input signal. Since the counter always counts up to 100 (leading edge of the input signal); the output state that exists upon detecting the trailing edge corresponds to the percentage of the pulse duration in relation to the



period. Example: assuming that the duty factor of the input signal is 60%, the counter is started at state 00 on the leading edge of the input signal, and is at state 60 when the trailing edge commences, so that '60' is latched and displayed. The latch pulse is generated with the aid of monostable IC<sub>1</sub> and timing parts R<sub>1</sub>-C<sub>1</sub>, while R<sub>22</sub>-C<sub>4</sub> ensure that the display does not flicker when the input frequency is equal or close to the sample frequency. Each display value is so retained for about 0.5 s. Switch S<sub>1</sub> selects between duty factor (position 2, 0-99%) and dwell angle readings (position 1, 0-90°). The latter scale is obtained by programming a divide factor, and hence a PLL multiplication factor, of 90 with the aid of NAND gates N<sub>3</sub>-N<sub>4</sub>. The input impedance of the duty factor analyser is 100 kΩ. Input signals should be at least 8 V<sub>pp</sub>: a suitable preamplifier set up with a switching transistor may be added to increase the sensitivity. Finally, it is recommended to fit the dashed diodes at the input of N<sub>1</sub> to afford protection against too high or reverse voltages.

D

#### Parts list

Resistors (± 5%):

R<sub>1</sub> = 10K  
R<sub>2</sub> = R<sub>15</sub> incl.; R<sub>21</sub> = 470R  
R<sub>16</sub> = 100K  
R<sub>17</sub> = 2K2  
R<sub>18</sub> = 470K  
R<sub>19</sub> = 47K  
R<sub>20</sub> = 33K  
R<sub>22</sub> = 1M5

Capacitors:

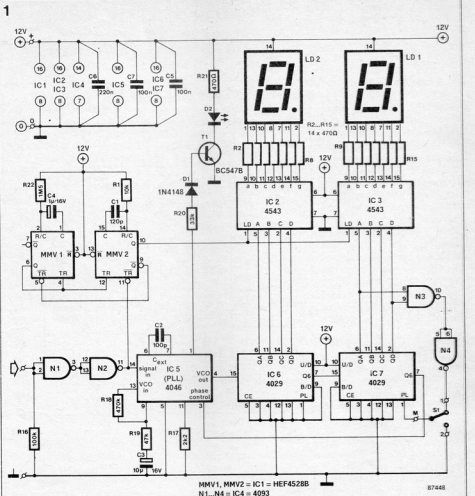
C<sub>1</sub> = 120p  
C<sub>2</sub> = 100p  
C<sub>3</sub> = 10 μ; 16 V  
C<sub>4</sub> = 1 μ; 16 V  
C<sub>5</sub>; C<sub>7</sub> = 100n  
C<sub>6</sub> = 220n

Semiconductors:

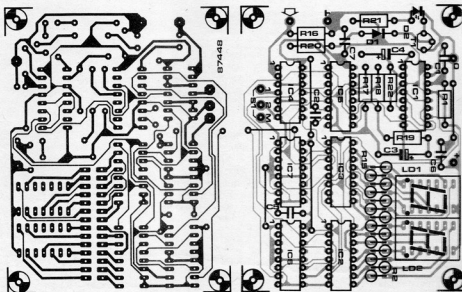
D<sub>1</sub> = 1N4148  
D<sub>2</sub> = LED green  
T<sub>1</sub> = BC547B  
IC<sub>1</sub> = 4528  
IC<sub>2</sub>; IC<sub>3</sub> = 4543  
IC<sub>4</sub> = 4093  
IC<sub>5</sub> = 4046  
IC<sub>6</sub>; IC<sub>7</sub> = 4029  
LD<sub>1</sub>; LD<sub>2</sub> = common anode type, e.g. 7651 or 7766.

Miscellaneous:

S<sub>1</sub> = miniature SPDT switch.  
PCB Type 87448 (see Readers Services).



2



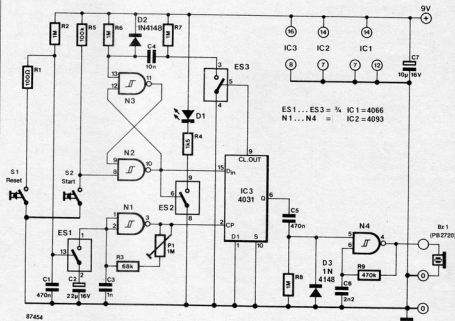
## 5

TIMER FOR  
FIXING BATH

by A Behrens

When, after developing, photographs are immersed in the fixing bath at irregular intervals, it becomes difficult to observe the correct fixing time for each of these. This problem is solved by the present timer, which is capable of "remembering" up to 32 immersion times, and automatically provides a signal when a photograph is to be taken out of the bath. Any time a photograph is immersed in the fixer, the user presses the start key on the timer, which responds by lighting a LED. When the fixing interval has lapsed, the timer provides a short beep.

The circuit is composed of a 64-stage shift register which is loaded with zeroes on power up, because it lacks a reset input. Electronic switch ES<sub>1</sub> connects the frequency determining capacitor to the input of clock oscillator N<sub>1</sub>. The logic level that exists at the D<sub>in</sub> terminal of IC<sub>3</sub> is shifted towards output Q at a speed that is defined by P<sub>1</sub>, which enables defining fixing times between roughly 1 and 10 minutes, 9 minutes being a commonly used value.



When the START button is pressed, S-R (set-reset) bistable N<sub>1</sub>-N<sub>2</sub> toggles, and LED D<sub>1</sub> lights. A logic 1 is written into the shift register with the aid of a positive pulse transition applied to terminal CP. After 64

clock pulses from N<sub>1</sub>, the logic high level is available at the output of the shift register, and enables oscillator N<sub>4</sub> to drive piezoelectric buzzer Bz<sub>1</sub>. The LED is turned off shortly after the START button is pressed,

because the bistable is reset by the CL. OUT pulse from IC<sub>3</sub>. The timer is conveniently fed from a 9 V battery, and should not consume more than about 10 mA.

Th

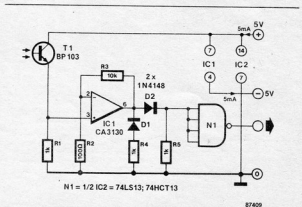
## 6

LIGHT  
DETECTOR

This circuit provides a computer with information about the presence of daylight. Possible applications include automatically measuring the duration of the daylight period in an autonomous weather station, or in control systems for outside lighting around the home. The computer can be programmed to monitor the output of the light detector, and automatically arranges for the relevant lights to come when it gets dark. The circuit is simple enough to enable ready construction on a piece of veroboard. Its output is

TTL compatible, and logic low when the phototransistor detects light. The sensitivity can be made adjustable for particular requirements by replacing R<sub>1</sub> with a series connected 10 KΩ preset and a 270 Ω resistor.

St



87409



# CURRENT CORRECTED AF AMPLIFIER

The majority of modern AF power amplifiers drive the loudspeaker(s) with a voltage that is simply a fixed factor greater than the input voltage. It is fairly evident, therefore, that the power delivered by such amplifiers is inversely proportional to the loudspeaker impedance, since the cone displacement of a loudspeaker is mainly a function of the current sent through the voice coil, whose impedance may vary considerably over the relevant frequency range. In multiway loudspeaker systems, this difficulty is overcome by appropriate dimensioning of the crossover filter, but a different approach is called for when there is but one loudspeaker. This amplifier is based on current feedback to ensure that the current sent through the voice coil remains in accordance with the input signal. The current through the voice coil and  $R_7$  develops a voltage across the resistor. A negative feedback

loop is created by feeding this reference voltage to the inverting input of IC<sub>1</sub>. The overall amplification of the circuit depends on the ratio of the loudspeaker's impedance,  $Z_L$ , to the value of  $R_7$ . In the present case the amplification is 16 times ( $Z_L/R_7 = 8/0.5 = 16$ ). The connection of the opamp's output to ground is slightly unusual, but enables the base current for output transistors  $T_1$ - $T_2$  to be drawn from the supply rails, rather than from the opamp. Capacitor  $C_6$  functions to set the roll-off frequency at about 90 kHz. The quiescent current of the amplifier is of the order of 50 to 100 mA for class A operation, and is determined by  $R_3$ - $R_4$  and  $R_5$ - $R_6$ . The complementary power transistors should be closely matched types to avoid fairly large offset currents (and voltages) arising. Some redimensioning of either  $R_3$  or  $R_4$  may be required to achieve the correct balance for the power

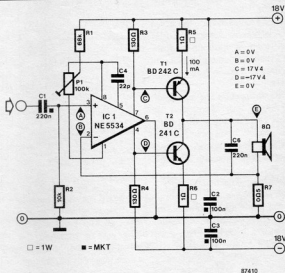
output stage. The emitter current of  $T_1$  and  $T_2$  is about 500 mA when the amplifier is fully driven.

The harmonic distortion of this

amplifier is less than 0.01% at  $P_o = 6.25$  W and  $U_b = \pm 18$  V.

Sv

Source: Texas Instruments  
Linear Applications.

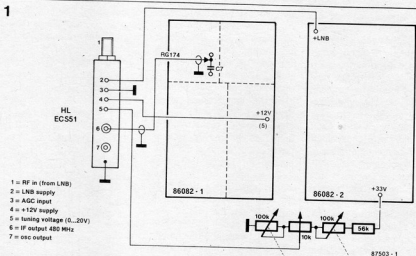


by R v Terborgh

The series of articles on satellite TV reception, started in the September 1986 issue of *Elektor Electronics*, has met a great deal of interest from our readers. Many have successfully ventured out into the world of centimetre waves and SHF construction methods, and are proud to watch the pictures produced by a home-made Indoor Unit <sup>(1)</sup>.

The construction and alignment of the RF input stage and the local oscillators is undoubtedly the most difficult phase of the project. However, an attractive alternative is now available for those constructors hesitant about their skills in dealing with very high frequency components and techniques. The Type HL ECSS1 is a ready-made, tunable, 950-1750 MHz to 480 MHz converter of Taiwanese origin, and is eminently suitable for taking over the previously mentioned functions on the RF board (Type EPS 86082-1). The module is tuned with a voltage between 0 and 20 V, and requires no band (H/L) switch. It has a connection for applying the LNB supply voltage, which is carried to the LNB via the download cable as usual. The module itself is conveniently fed from 12 VDC, and consumes about 100 mA. Its RF input is a Type F socket.

Figure 1 shows the ready connection of the module to the RF board in the IDU. Module pin 3 is the AGC input, which is grounded here to achieve maximum gain. A 56 k $\Omega$  resistor is fitted in series with the existing +33 V tuning voltage rail to ensure the correct maximum input to pin 5. The IF output on the module accepts a common phono plug, to which a short length of thin (RG174) coax cable is soldered for connecting to the short track between pin 3 and 4 of MX<sub>1</sub> on the RF board. Coupling capacitor C<sub>7</sub> should be left in place, but MX<sub>1</sub>, the RF input stage, and both local oscillators may be omitted, since the module takes over their function. In case the



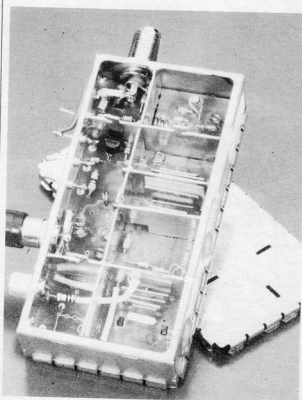
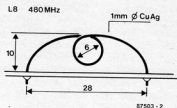
RF board is already complete, it is recommended to remove MX<sub>1</sub>, R<sub>3</sub> and band selector S<sub>1</sub>. The screen between the RF input stage and the local oscillators may also be omitted, but not the remaining screens on the board.

Before aligning the "modular" Indoor Unit, the intermediate frequency requires lowering from 610 to 480 MHz. The VCO in the SL1451 PLL can be tuned to the new centre frequency by increasing the inductance of L<sub>8</sub>. This is easiest to do by making a new inductor as shown in Fig. 2. Use about 5 cm of silver plated,  $\varnothing$  1 mm (SWG20) wire to make the single turn inductor, ensuring that the underside of it is just above the PCB surface.

The alignment procedure of the module-based Indoor Unit is essentially identical to that set forth on page 54 in Part 2 of <sup>(1)</sup>. The reference there to TV channel 36 (600 MHz) should then be read as TV channel 21/22 (approx. 480 MHz). The IF band-pass filters can be tuned to the new frequency when the respective trimmers are set for nearly maximum capacitance.

Finally, a note on the results obtained with the module in combination with the RF board as described here: the original, completed, and properly aligned RF board with the BFG65, local oscillators, and MX<sub>1</sub> fitted gives a slightly better performance when relatively

2



weak signals ( $C/N \leq 12$  dB) are being received. This is mainly due to its noise figure being lower than that of the HL ECS51 module, which is specified for

no less than 15 dB in this respect. None the less, the module gives good results with relatively strong input signals.

RGK

The HL ECS1 module is available through Bonex Limited • 102 Churchfield Road • Acton • London W3 6DH. Telephone: (01 992) 7748 or (01 993) 7631.

**Literature reference:**

(1) Indoor Unit for Satellite TV Reception Parts 1-3; *Elektronika*, October 1986 and following issues.

# 10

## BIDIRECTIONAL SERIAL-PARALLEL CONVERTER

by R. Baltissen

This interface circuit enables doing rather more than normally possible with the computer's serial (RS232) port. Serial output data from the computer is converted into parallel format, and parallel data applied to the interface is converted into a serial bit stream for reception by the computer.

The interface is based on the industry standard UART (universal asynchronous receiver/transmitter) Type AY-5-1013, or the CMOS version of it, the CDPI854 from RCA. Serial data from the computer is received at input RXD, and inverted in T<sub>1</sub> for driving the RSI input on the UART, which converts the received word into 8-bit parallel format (RD<sub>0</sub>-RD<sub>7</sub>). The shifting in of serial bits is clocked by the 19,200 Hz signal applied to the RCP and TCP input. This fixes the baud rate of the interface at 1200 (19,200/16). The baud rate generator is a conventional design based on a binary counter/divider with built-in clock oscillator, which is crystal controlled here and operates at 2.4576 MHz. The parallel output of the UART is buffered with the aid of IC<sub>2</sub> to enable controlling 8 relay drivers B<sub>1</sub>-B<sub>8</sub>. The parallel word applied to the UART at its TD<sub>0</sub>-TD<sub>7</sub> inputs is converted into serial format and output via the TSO terminal, where the signal is inverted and fed to the TXD output.

The serial data format can be defined with the aid of wire links B-F; Table 1 lists the function of each of these. Inverter T<sub>2</sub> automatically resets the receiver in the UART by driving RDAR (received data available reset) low when RDA (received data available) goes high to signal that a complete word has been shifted into the receiver hold register. When wire link A

is installed, RDA can also control the TDS (transmitter data strobe) input, so that a new parallel word (TD<sub>0</sub>-TD<sub>7</sub>) is loaded into the transmitter holding register. Thus, jumper A makes it possible to use the CTS (clear to send) handshaking signal. The TEOC (transmitter end of character) pulse is used here to generate the RTS handshaking signal, and also to control the TDS input, together with CTS. This handshaking input, when active, prompts the UART to output a new serial word. Set-reset bistable N<sub>1</sub>-N<sub>2</sub> precludes conflicts arising between the

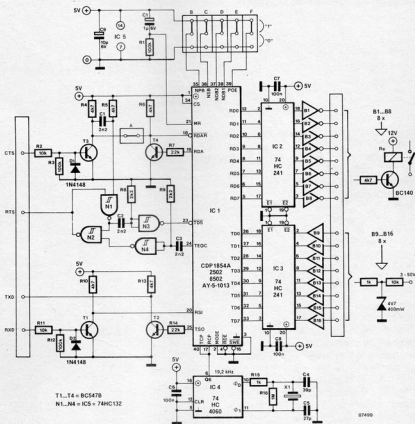


Table 1

link	fitted	not fitted
A	no RTS & CTS	RTS & CTS
B	no parity bit	parity bit
C	2 stop bits	1 stop bit
D/E	see below	
F	even parity	odd parity
D	E	data word
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

signals in question. Power-on network C<sub>1</sub>-R<sub>1</sub> ensures that the UART is properly reset and initiated. TSO and TEOC then go high, while RDA is forced low. When link A is not fitted, the presence of the inverted TEOC pulse at input TDS causes the transmission process to commence.

The author has developed this circuit mainly to enable two IBM PCs to communicate with the aid of the Turbo Pascal program listed in Table 2. Before this can be run, the status of serial port COM1:

(AUX:) should be defined by typing DOS command  
MODE COM1:1200,n,8,2 <CR>  
(1200 baud, no parity, 8 data bits and 2 stop bits).

Pins 6 (DSR) and 20 (DTR) on the 25-way D socket should be interconnected, and the same goes for pins 4 (RTS) and 5 (CTS) when no handshaking is being used. When it is intended to use the handshaking facility on the bidirectional interface, link A should be removed, and socket pins 4 and 5 connected to interface terminals CTS and RTS respectively.

Sv

Table 2

```
var n : integer;
    v : char;

begin
  repeat
    n := 0;
    repeat
      write(aux,chr(n));
      read(aux,v);
      write(ord(v),' ');
      n := n+1;
      delay (500);
    until (n = 256) or (keydepressed = true)
  until keydepressed = true
end
```

# 11

## INTEGRATED STEREO AMPLIFIER

The Type TDA1521 from Valvo/Mullard is an integrated HiFi stereo power amplifier designed for mains fed applications such as stereo TV. The device works optimally when fed from a  $\pm 16$  V supply, and delivers a maximum output power of  $2 \times 12$  W into  $8 \Omega$ . The gain of the amplifiers is fixed internally at 30 dB with a spread of 0.2 dB to ensure optimum gain balance between the channels.

A special feature of the chip is its built-in mute circuit, which disconnects the non-inverting inputs when the supply voltage is less than  $\pm 6$  V, a level at which the amplifiers are still correctly biased. This arrangement ensures the absence of unwanted clicks and other noise when the amplifier is switched on or off. The TDA1521 is protected against output short circuits and thermal overloading. The SIL9 package should be bolted onto a heat-sink with a thermal resistance of no more than  $3.3$  K/W ( $R_{th} = 8 \Omega$ ;  $V_s = \pm 16$  V;  $P_d = 14.6$  W;  $T_A = 65^\circ$  C). Note that the metal tab on the chip package is internally connected to pin 5.

The accompanying photograph shows that this high quality stereo amplifier has a very low component count, and is readily constructed on a piece of Veroboard.

Distortion at  $P_o = 12$  W:

0.5%

Quiescent current:

40 mA

Gain balance:

0.2 dB

Supply ripple rejection:

60 dB

Channel separation:

70 dB

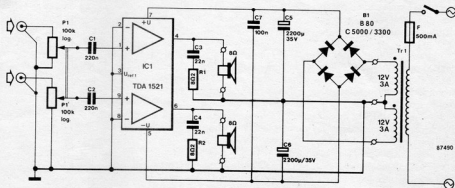
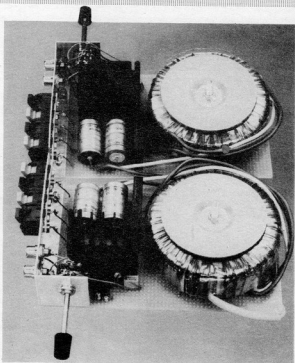
Output offset voltage:

20 mV

3 dB power bandwidth:

20-20,000 Hz

R





from an idea by M Wiegiers

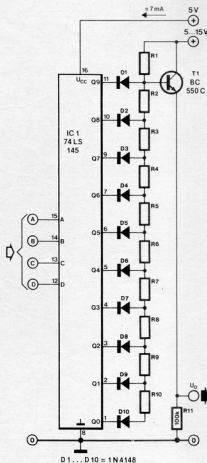
Two simple to build 4-bit digital-to-analogue converters are described here. One translates a 4-bit BCD code into 10 analogue voltage levels, the other accepts a 4-bit binary code and outputs 16 voltage levels. Both circuits comprise a digital decoder with open collector outputs for controlling a resistance ladder. The analogue voltage is obtained by controlled connection to ground of a particular section of the ladder, and buffering the drop so obtained with a transistor.

Notwithstanding their relatively low resolution (10 or 16 steps), the circuit should have many possible applications, including driving digitally controlled power supplies, triangular wave and sawtooth generators, and A-D converters.

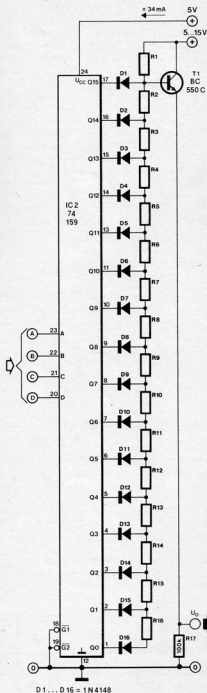
Table 1 lists the relative values of the resistors in the ladder network, starting from  $R_1 = 1K\Omega$ . Three values are given for each resistor: the left-hand column shows the theoretical value, while the nearest equivalent from the E24 and E96 series appears in the centre and right hand column, respectively. Note that the starting value can be changed to individual requirements, provided all other resistors are dimensioned accordingly, i.e., their values should be multiplied with the same factor with respect to  $1K\Omega$ . It is a relatively simple matter to add an 11th or 17th output level by driving the decoder such that none of its output transistors is enabled. This results in an output voltage which is 0.6 V lower than the supply for the ladder network. In the case of the 74LS145, this condition is obtained by applying a non-valid code to the inputs, i.e., one greater than  $9_{10}$  ( $1001_2$ ). Similarly, on the 74159, enable input G1 or G2 can be made logic high.

SV

$R_n$	10-step BCD version			16-step binary version		
$R_1$	1000	1K0	1K0	1000	1K0	1K0
$R_2$	111	110	110	66.7	68	66.5
$R_3$	139	130	140	76.3	75	76.8
$R_4$	179	180	178	87	91	86.6
$R_5$	238	240	237	103	100	102
$R_6$	333	330	332	122	120	121
$R_7$	500	510	499	145	150	147
$R_8$	833	820	825	178	180	178
$R_9$	1667	1K6	1K69	222	220	221
$R_{10}$	5000	5K1	4K99	286	270	287
$R_{11}$				381	390	383
$R_{12}$				533	510	536
$R_{13}$				800	820	806
$R_{14}$				1333	1K3	1K33
$R_{15}$				2667	2K7	2K67
$R_{16}$				8000	8K2	8K06



D1...D10 = 1N4148



D1...D16 = 1N4148

87418

Many modern AF power output stages are capable of delivering considerable power levels in the supersonic frequency range. When the loudspeaker can not handle that power, the voice coil is rapidly overheated, and causes a short-circuit. If the power output stage is not properly protected, it breaks down and supplies a direct current that effectively destroys the loudspeaker.

The present loudspeaker protector is composed of three sections: a measuring amplifier, a detector, and a relay driver. Four channels are shown here as an example. Potential divider  $R_1$ - $R_2$  determines the sensitivity of the protection circuit, while  $D_1$ - $D_2$  protect the input of  $A_1$ . Opamp  $A_3$  is set up as a low pass filter with a cut-off frequency of 0.5 Hz, so that it can

function as a DC detector. The second section of the circuit is composed of four detectors  $A_5$ - $A_{12}$ .  $A_5$  compares any negative direct voltages to a reference set with  $R_8$ - $R_9$ , while  $C_3$ - $R_7$  determine the delay time. Opamp  $A_{10}$  has a similar function for positive direct voltages. The circuit is actuated when

$$\frac{V_{in}R_2}{R_1+R_2} - 0.65 > \frac{15R_2}{R_8+R_9}$$

Comparators  $A_{11}$  and  $A_{12}$  function as the power limiter. Positive and negative peak voltages are rectified in  $D_3$ - $D_4$  and averaged with the aid of R-C combinations  $R_{10}$ - $C_{13}$  and  $R_{16}$ - $C_{15}$ . The relatively long periods of these networks precludes erroneous triggering of the circuit on peaks in the input signal.

The power limiter is actuated when

$$\frac{V_{in}R_{21}/2}{R_{11}+R_{12}} - 0.65 > \frac{15R_{20}}{R_{28}+R_{29}}$$

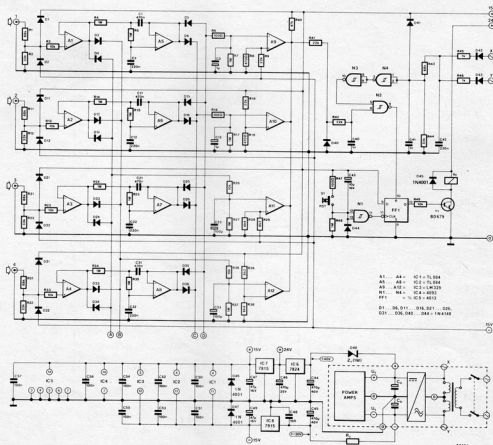
This equation is also valid for the positive detector set up around  $A_{12}$ . The stated component values result in  $P_{max} \approx 30$  W in  $8\Omega$ .

When the input signals are all right, the open collector outputs of  $A_5$ - $A_{12}$  are in their high impedance state, so that the output voltage is +15 V via  $R_{46}$ . When a fault condition exists at one or more of the inputs, junction  $R_{46}$ - $R_{41}$  is pulled down to -15 V.

The central part in the relay driver is bistable FF. Gate  $N_1$  is a resettable power-up delay circuit which clocks FF. The logic high level at the D (data)

input is only transferred to output Q when the R (reset) input is logic high. It is seen that a reset pulse can originate either from the mains detector  $N_3$ - $N_4$ , or from the fault detectors  $A_5$ - $A_{12}$ . The loudspeaker protector is conveniently fed from the amplifier's symmetrical supply, but care should be taken to dimension  $D_{48}$  and  $R_7$  such that the indicated voltage across  $C_{44}$  and  $C_{45}$  is not exceeded. If the amplifier supply delivers less than 28 V,  $IC_6$  may be omitted, and the loudspeaker relay, Re, replaced with a 12 V type fed from the +15 V rail. Voltage divider  $R_{43}$ - $R_{44}$  should then be redimensioned such that the input of  $N_4$  is held at about +13 V when  $R_{43}+R_{44} \approx 100$  k $\Omega$ .

Sv



There is little doubt that the headphone amplifier described here belongs in the so-called *high end* class of audio equipment, and is, therefore, perfect for incorporation in, or adding to, the *Top-of-the-range Preamplifier* described in <sup>11</sup>, although it is also suitable as an autonomous, high quality, unit. The circuit diagram of the headphone amplifier appears in Fig. 1. The unit is based on Type OP-50 power operational amplifiers, whose technical features are summarized in Table 1. Clearly, everything feasible has been done by the manufacturers, Precision Monolithics Inc., to ensure optimum operation of the device, and it is with this in mind that the remainder of the amplifier was designed.

Both supply rails to the amplifier ICs are adequately decoupled and filtered with a small series resistor ( $R_1$ ,  $R_1'$ ) and a combination of an electrolytic and a solid capacitor ( $C_1$ ,  $C_2$  and  $C_3$ ,  $C_3'$ ). With reference to the upper of the two identical channels, preset  $P_2$  enables compensating the (small) offset voltage at the output of the OP-50, while  $C_1$ - $R_3$  forms a compensation circuit to minimize overshoot for a given closed-loop voltage amplification,  $AV_{CL}$ . In the present application,  $AV_{CL}$  is about 6, since

$$R_1 = R_2 / (AV_{CL} - 1)$$

When it is intended to alter the amplification,  $R_2$  should be left at 20 k $\Omega$ . Also observe that the indicated values for  $R_3$  and  $C_1$  are valid when  $AV_{CL}$  is between 5 and 20, while  $R_3 = 3.3$  k $\Omega$  and  $C_1 = 1$  nF when  $AV_{CL}$  is between 20 and 50. No R-C compensation is required when  $AV_{CL}$  is greater than 50.

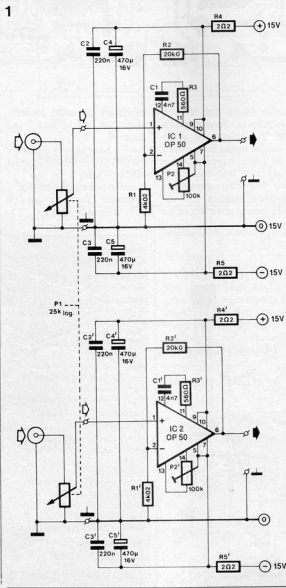
The +15 V supply for the headphone amplifier is a relatively extensive circuit based on a precision regulator Type LM325, which features excellent noise suppression whilst ensuring smooth and simultaneously rising output voltages

#### OP-50 Power operational amplifier

##### Features:

- Open-loop gain: 10<sup>6</sup> V/V min.
- Input offset voltage: 25  $\mu$ V max.
- Input bias current: 5 nA max.
- Offset voltage drift: 0.3  $\mu$ V/ $^{\circ}$ C max.
- Common mode rejection ratio: 126 dB min.
- Power supply rejection ratio: 126 dB min.
- Noise level: 5.5 nV/ $\sqrt{\text{Hz}}$  ( $f = 10$  kHz)  
4.5 nV/ $\sqrt{\text{Hz}}$  ( $f = 1$  kHz)  
 $\pm 50$  mA
- Output current:  $\pm 50$  mA
- Drives capacitive loads up to 10 nF.
- On-chip thermal shutdown circuit.

Data taken from manufacturer's data sheet.

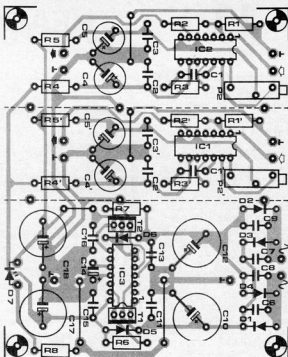
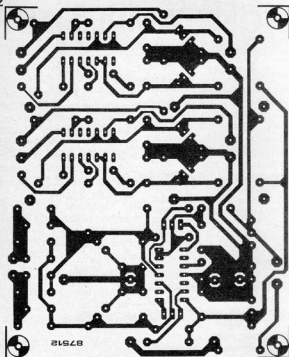


at power-on. Mains-borne interference and clicks from  $S_1$  are suppressed in varistor  $R_3$  and high-voltage capacitor  $C_5$ . The four diodes in rectifier bridge  $B_1$  are bypassed with rattle suppression capacitors to ensure minimum noise on the supply rails to the opamps.

The headphone amplifier can function optimally only if great care is taken both in the choice of the components and in the construction on PCB Type 87512, details of which are shown in Fig. 2. As already stated, the headphone amplifier is suitable for building into the Top-of-the-Range Preamplifier. This makes it possible to feed the  $\pm 15$  V regulator from the raw voltage across  $C_5$  (+) and  $C_{10}$  (-) of the existing  $\pm 18.5$  V supply, while the inputs of the volume control of the headphone amplifier are driven direct from the outputs of  $IC_4$  (R) and  $IC_4'$  (L).

Opamps  $IC_1$  and  $IC_2$  should be soldered direct onto the PCB, and are preferably fitted with a DIL-type heatsink. Provision has been made to screen the amplifiers and the supply on the board by means of two sheets of brass or tin plate, which are mounted vertically onto the dotted lines, and secured with three soldering pins each. Series regulators  $T_1$  and  $T_2$  can do without a heat-sink. When the board is complete, its underside should be thoroughly cleaned with a brush dipped into white spirit or alcohol to remove any residual resin. Next, the track side is sealed with a suitable plastic spray.

When possible, use insulated sockets for the stereo input and output of the amplifier. At the input side, few problems are expected to arise when using gold-plated phono sockets mounted onto a separate ABS or epoxy plate. When a good quality, insulated, 6.3 mm, stereo headphone socket proves unobtainable, the nearest alternative is a non-insulated type, whose common tag is connected direct to the ground point on the PCB, between  $C_{17}$



and  $C_{18}$  to effect central earthing. Mains transformer  $Tr_1$  is preferably a toroidal type fitted behind a metal screen to ensure minimum hum and other interference picked up by the amplifier inputs. Presets  $P_2$  and  $P_1$  are trimmed for minimum offset voltage at the respective

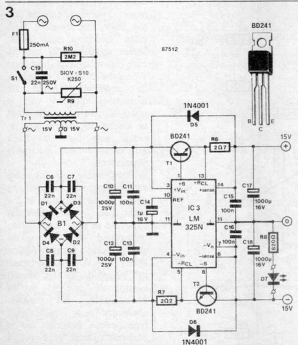
amplifier's output—this is likely to require a very sensitive DMM. The headphone amplifier can be terminated in  $100\ \Omega$  to  $1\ k\Omega$ , and is therefore perfect for use as a high-quality line driver also. The outputs are short-circuit resistant. Finally, a brief summary of the

amplifier's expected performance at  $V_o = 6\ V_{rms}$  and  $Av_{cl} \approx 6$ :  
Total harmonic distortion: 0.0025% (100 Hz); 0.003% (1 kHz); 0.011% (0 kHz).  
Signal-to-noise ratio:  $\geq 80\ dB$   
Response flatness:  $\pm 0.4\ dB$  from 10 Hz to 20 kHz.

Sv

#### Literature references:

- (1) *Top-of-the-Range Preamplifier*. Elektor Electronics, November and December 1986, January 1987.
- (2) *Linear and Conversion Applications Handbook (1986)*. Precision Monolithics Incorporated.



#### Parts list

- Resistors ( $\pm 5\%$ ):  
 $R_1, R_1' = 4K02F^*$   
 $R_2, R_2' = 20K0F$   
 $R_3, R_3' = 560R$   
 $R_4, R_4', R_5, R_5', R_6, R_7 = 2R2$   
 $R_8 = 820R; 0.5\ W$   
 $R_9 = S10V\ S10\ K250$  varistor  
 (Siemens; ElectroValue (0784) 33603).  
 $R_{10} = 2M2$   
 $P_1 = 25K$  logarithmic stereo potentiometer.  
 $P_2, P_2' = 100K$  multiturn preset.  
 Capacitors:  
 $C_1, C_1' = 4n7$   
 $C_2, C_2', C_3, C_3' = 220n$   
 $C_4, C_4', C_5, C_5' = 470\mu; 16\ V$ ; radial  
 $C_6, C_7, C_8, C_8' = 22n$   
 $C_9, C_9' = 1000\mu; 25\ V$ ; radial  
 $C_{10}, C_{10}', C_{11}, C_{11}' = 100n$   
 $C_{12} = 1\mu; 16\ V$ ; tantalum  
 $C_{13} = 22n; 250\ VAC$   
 $C_{14}, C_{14}' = 1000\mu; 16\ V$ ; radial  
 Semiconductors:  
 $D_1 \dots D_6$  incl. = 1N4001

$D_7$  = LED red  
 $IC_1, IC_2$  = OP-50 (Precision Monolithics Inc.)  
 $IC_3$  = LM325  
 $T_1, T_2$  = BD241

#### Miscellaneous:

- $F_1$  = 250 mA delayed action fuse plus panel-mount holder.  
 $Tr_1$  =  $2 \times 15\ V; 15\ VA$  ( $\approx 2 \times 0.50\ A$ ) toroidal mains transformer, e.g. ILP Type 03013. Jaytec, (0227) 375254.  
 DIL-14 heat-sink for  $IC_1$  and  $IC_2$ .  
 Mains entrance socket.  
 PCB Type 87512 (available through the Readers Services).  
 $S_1$  = SPST miniature mains switch.  
 Stereo 6.3 mm headphone socket, preferably insulated.  
 2 off phone input sockets.  
 Suitable metal enclosure.

\* See text

\* Contact Audikits Precision Components (see page 62).



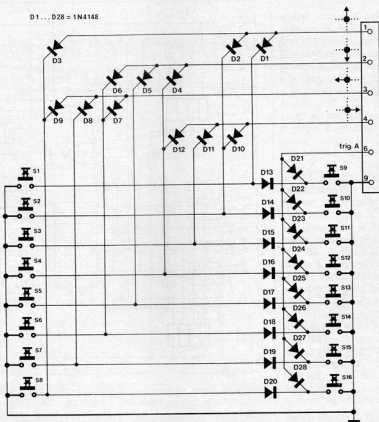
This simple circuit is an unusual, but interesting, application of the joystick port available on an MSX microcomputer. With some modifications, it should also work with other types of computer equipped with a similar "game" input. The use of the joystick port for reading 16 switches is advantageous because very little additional hardware is required, and programmers can avail themselves of standard BASIC instructions relating to the joystick.

On MSX computers, the position of the joystick handle is read with the aid of instruction **STICK(n)**, where *n* is 1 or 2, i.e., the number of the relevant joystick. The instruction returns an integer between 1 and 8, from which the handle position is deduced as shown in Fig. 1. Instruction **STRIG(n)** enables determining the state of the trigger (fire) button on joystick *n*, and returns -1 when this is actuated.

A diode matrix is used here to enable connecting eight pushbuttons *S1-S8* to the four direction inputs on the joystick port. When actuated, either one of these buttons forces a logic low level upon one or two of the input lines, enabling the computer to identify the key number. Eight additional diodes, *D1-D8*, make it possible to double the number of keys (*S9-S16*). These can be kept distinct from the former 8 by connecting them to the trig. A input.

The 16 keys are identified in

2



BASIC with the aid of instructions

$X = \text{STICK}(1)$  (or  $X = \text{STICK}(2)$ ) and

$Y = \text{STRIG}(1)$  (or  $Y = \text{STRIG}(2)$ ) so that the key number is simply

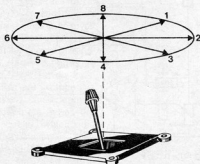
$Z = X - (Y * 8) + 1$ .

This goes to show how a versatile extension can make good use of existing hardware whilst being controllable with BASIC commands. Finally, Fig. 3 shows the pin assignment on

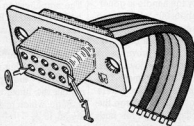
the 9-way sub D connector used for connecting the present circuit to the MSX joystick port.

R

1



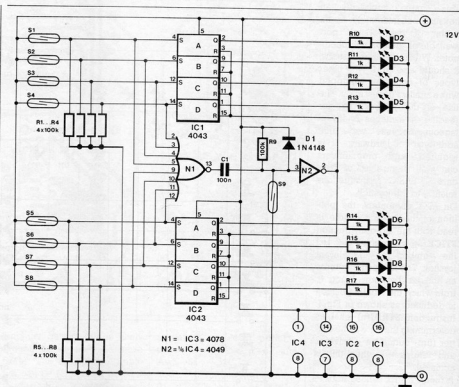
3



By E J Carroll

This section indication system may be a just the thing you have been looking for when you own a fairly large model railway with tunnels and tracks at several levels, and are sometimes at a loss find the whereabouts of a particular train. This circuit uses LEDs to indicate the train's position. Each track block is split up into 8 sections, whose starting points are marked with reed contacts ( $S_1$ - $S_8$ ). A ninth reed contact is fitted at the end of the block, to enable turning off the indication for the relevant length of the track.

The circuit is composed of 8 set-reset (S-R) bistables, which drive a LED each. All SET inputs are combined in a NOR gate,  $N_1$ , which drives a pulse shaper and buffer to reset the bistables with a brief pulse to ensure that only the LED for the last passed track section is lit. The reed contacts are actuated with the aid of a small magnet fitted to the underside of the engine. Depending on the most suitable location of the magnet, the reed contacts are fitted in between the tracks or alongside the left or right hand rail.

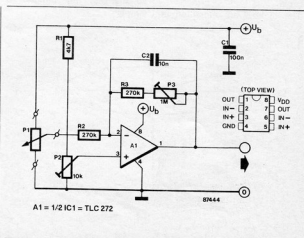
LEVEL ADAPTOR FOR  
ANALOGUE JOYSTICK

An analogue joystick usually contains two potentiometers, whose wipers are controlled from the central handle on the unit. Unfortunately, the angle covered by the handle is generally only about  $90^\circ$ , whereas the potentiometer's spindle and wiper can be rotated over  $270^\circ$ . The voltage range provided by a potentiometer in a joystick is, therefore, relatively small. Two of the circuits described here make it possible to enlarge the output voltage range of both potentiometers in the joystick. The circuit is readily doubled, thanks to the use of dual CMOS operational amplifier Type

TLC272.

Each of the two wiper voltages from the joystick is processed separately, which enables interesting effects to be achieved. The amplification of the circuit is determined by  $P_3$ . This preset enables the enlarging of the potentiometer's "range" to individual requirements. Preset  $P_2$  serves to shift the operative range of the potentiometer within the limits of the supply voltage, which may lie between 3 and 16 V.

Setting up this circuit is straightforward. Commence with setting  $P_1$  for minimal resistance, i.e.,  $A_1$  should give unity gain.



Set the joystick handle to its centre position, so that the wiper of  $P_1$  is at mid-travel. Adjust  $P_2$  to make the output voltage of the circuit equal to  $\frac{1}{2}V_{dd}$ . Move the joystick handle to the outer positions in the relevant plane, and note the corre-

sponding output voltages from the circuit. Adjust  $P_1$  such that the circuit outputs the required voltage span. The adjustment of  $P_2$  enables changing the toggle point of the circuit, that is, the voltage it outputs when the joystick handle is set to its

centre (rest) position. The current consumption of the circuit depends on the supply voltage level, and also on the value of  $P_1$ . When  $V_{dd}=5$  V, and  $P_1=4$  K $\Omega$ , the current drain is less than 10 mA. The Type TLC272 was chosen because it

works fine from a single supply voltage, and also because it has an extensive input voltage range, 0 to  $V_{dd}-1.5$  V.

Th

## 18

## 6-WAY CHANNEL SELECTOR

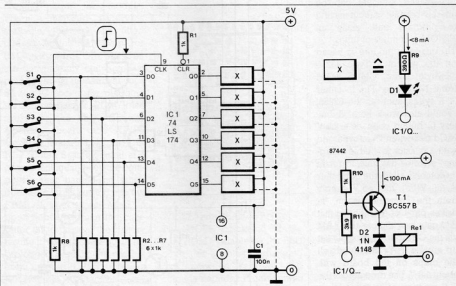
by U Günther

This design proves that a latching 6-way channel selector with debounced switch inputs need not always be based on the use of special integrated circuits.

When none of the break-type SPDT push buttons is pressed, the data inputs of IC<sub>1</sub> are held at +5 V, while input CLK is held low via  $R_8$ . When a switch is operated, the associated input of IC<sub>1</sub> goes low, while CLK goes high, so that the logic state of the De-Dr lines is latched and transferred to outputs  $Q_0$ – $Q_5$ . Each of these can drive a LED or relay based output circuit as shown.

When more than six switches are required, a 74LS174 may be added, whose clock input is connected to IC<sub>1</sub>.

Note that the LS chip may be replaced by a corresponding



version from the HC or HCT family. This will reduce the cur-

rent consumption from about 20 mA to 6 mA. The maximum

output current supplied by IC<sub>1</sub> is 8 mA in all cases.

W

## 19

## TOILET POINTER

by R Kambach

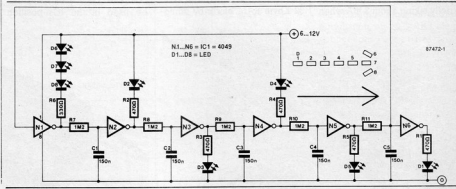
It often happens on parties that numerous guests are at a loss in finding the toilet, and politely but urgently require to be given directions to that effect. The present pointer should be helpful to many, since it captures the attention by successively lighting LEDs that are arranged to form an arrow. The circuit is based on a single Type 4049 integrated circuit, which contains six CMOS inverters. Each of these has an R-C network at its output to ensure an appropriate delay before enabling the next inverter. The outputs of

the chip are capable of driving one LED direct, although some heating is expected to arise

from this. The circuit is conveniently fed from a PP3 (9 V)

battery, and consumes a mere 50 mA.

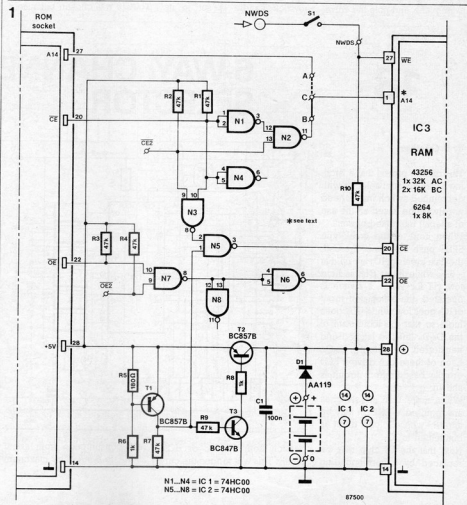
Th



This versatile, exchangeable, memory module should appeal to programmers developing software for computers other than the one being used for writing, testing and debugging the program. The battery back-up function of the module ensures that data is retained, and so makes it possible to use "portable", software that is ROM-based and yet can be altered readily without having to program and erase an EPROM a number of times.

The memory module is based on the use of a Type 43256 32 Kbyte static CMOS RAM from NEC—see Fig. 1. Other 32 K types, such as the 62256, should also work here. A battery (2 button cells, or a 2.4 V NiCd cell when D<sub>1</sub> is bypassed with a resistor to enable charging) enables the chip to retain its contents when the computer is off. When the +5 V supply from the computer is on, T<sub>1</sub> drives pin 1 of N<sub>3</sub> high, so that this gate can enable the RAM via the CE input. The supply set up around T<sub>1</sub>, T<sub>2</sub> then feeds all the chips on the board with about 4.8 V. The drop across the C-E junction of T<sub>2</sub> is less than 0.2 V here since the transistor is driven into saturation. When the computer is switched off, the circuit is fed from the battery via germanium diode D<sub>1</sub>. Voltage divider R<sub>3</sub>-R<sub>4</sub> causes T<sub>1</sub> to be turned off when the supply level drops below some 4.5 V.

Input 1 of N<sub>2</sub> is grounded via R<sub>7</sub>, so that CE on the RAM is held high, causing the chip to switch to the power-down (standby) mode. A prototype of the plug-in RAM consumed only 1.5 µA in the data retention mode, after briefly taking about 3 mA when



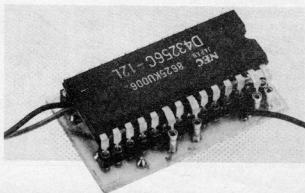
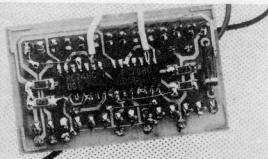
the input voltage dropped from 1.5 to 1 V. This effect is normal, however, and is due to the inputs of the HC gates briefly being in an undefined state. The ICs fitted were Types 74HC00 (SMD) and a 43256C-12L (120 ns).

The module is configured as a 32 Kbyte RAM block by fitting

wire jumper A-C, while jumper B-C selects 2 x 16 Kbyte. The latter configuration is required when the socket that receives the module is intended for a maximum memory capacity of 16 Kbyte (ROM or RAM), as on the BBC sideways extension board. A Type 6264 RAM can be used in the IC<sub>3</sub> position

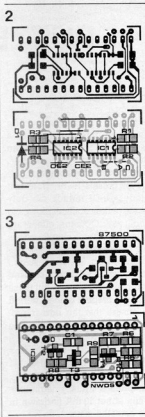
when only 8 Kbytes are required. Neither jumper need then be fitted.

Successfully constructing the RAM module requires great care in soldering the SMA parts onto the board shown in Fig. 2. It is absolutely necessary to first fit all the SMA parts at both sides of the board, then the



three wire links and jumper B-C or A-C as required. Do not forget to solder the terminals of D<sub>1</sub> (not an SMA part), and the battery connections, at both sides of the board. Also, through-contacting with short lengths of component wire should be effected at four locations. Push all the pins of two 14-way IC terminal strips through the straight rows of holes on the component side of the board, i.e. the side that holds the transistors, then solder the pins to the islands on the copper side, i.e., the side that holds the 74HC00s. The pins should protrude at least 4 mm. The use of a centrally cut wire-wrapping socket is not recommended here in view of the thickness of the pins. Locate the pin that protrudes from the hole marked 1, and cut it off. Mount a turned IC pin holder next to pin 28, 27, 22 and 20 of the right-hand side terminal strip, and solder these at both sides of the PCB. These pins should not protrude at the copper side, and their tops should be 1.5 to 2 mm above those in the terminal strip. When it is intended to use the RAM in its 2 x 16 Kbyte configuration, wires are connected to points OE2 and CE2 at the copper side, and guided between pins 5-6 and 9-10 respectively. Remove pin 1 of a standard 28-way IC socket, before carefully push-

fiting this onto the 27 protruding pins at the copper side. Connect the battery supply wires and the wire to S<sub>1</sub> (NWDS) to the respective points at the component side. Use a pair of precision pliers to carefully bend pins 28, 27, 22 and 20 of the 43256 or 6264 slightly to the right of the other pins in the row. This enables pushing these four IC pins in the previously mentioned, separate, socket pins, while the 24 others are inserted in the usual manner. The battery is conveniently mounted at some distance from the module. When a miniature battery is available, this can be fitted underneath the RAM chip. For BBC users: wires OE2 and CE2 are conveniently connected to pins 22 and 20 respectively of a 28-way IC socket for plugging into the adjacent ROM/RAM socket on the BBC's sideways extension board; the NWDS signal is available at pin 8 of IC<sub>1</sub>. Switch S<sub>1</sub> is mounted at a convenient location on the computer's rear panel, and when opened inhibits writing into the RAM. It is recommended to open S<sub>1</sub> after turning the computer off to prevent the battery having to supply some 50  $\mu$ A for prolonged periods: this current flows into the NWDS driver via R<sub>10</sub>. Non-BBC or Eletron Plus-1 users should note that the NWDS signal is the same as



WRITE, not READ/WRITE. The MOVE command in the ADT ROM available for the BBC computer enables exchanging data between resident and sideways memory. Programmers should have little difficulty, however, in writing a short

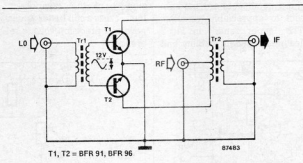
- Parts list**
- Note: all parts Surface Mount Assembly types unless marked \*.
- Resistors:  
R<sub>1</sub>...R<sub>4</sub> incl.; R<sub>7</sub>; R<sub>8</sub>; R<sub>10</sub> = 47K  
R<sub>5</sub> = 180R  
R<sub>6</sub>; R<sub>9</sub> = 1K0
- Capacitor:  
C<sub>1</sub> = 100n or 47n
- Semiconductors:  
D<sub>1</sub> = AA119 \*  
T<sub>1</sub>; T<sub>2</sub> = BC857B or similar pnp SMA type.  
T<sub>3</sub> = BC847B or similar npn SMA type.  
IC<sub>1</sub>; IC<sub>2</sub> = 74HC00 (Do not use HCT types).  
IC<sub>3</sub> = 43256C-10/12/15L (NEC) or 62256 LP10/12 32Kbyte CMOS static RAM \*.
- Miscellaneous \*:  
PCB Type 87500 (see Readers Services page)  
2 off 14-way terminal strips with 7 mm pins.  
4 off turned pins for IC leads.  
Suitable battery (see text, V<sub>b</sub>  $\geq$  2.4 V)

routine that selects the relevant sideways socket(s) via the socket latch at FE3Fh, and copying one or two 16 Kbyte blocks. *It is regretted that information on software for this project is not available.* (Ed.)

# 21

## HIGH LEVEL PASSIVE DBM

The mixer is one of the most important sections in any good-quality SW receiver, since it determines to a large extent the sensitivity and the dynamic range. The so-called switching mixer is often used, because it has none of the technical imperfections of active mixers. The most commonly found switching mixer is the diode-based double balanced type (DBM), which is, unfortunately, a notoriously expensive component, especially when a high intercept point is required to ensure low levels of intermodulation. The application of active devices, such as bipolar transistors and J-FETs, in a passive



mixer is less well established. And yet, these components enable the mixer to remain relatively simple, since the RF input signal can be thought of as electrically insulated from the local oscillator output. The

present design is based on a pair of well-known UHF transistors, which require no supply voltage or bias circuits. The input and output transformers are wound on two-hole ferrite cores (Baluns). The

primary of Tr<sub>2</sub> is 8 turns with a centre tap for the RF input, the secondary is 4 turns. Tr<sub>1</sub> is wound such that the indicated LO amplitude is available at the secondary. Only the RF input or the IF output requires correct termination on 50  $\Omega$ , the other connections are then fairly uncritical. The input intercept point of this mixer is excellent at between 31 and 36 dBm, while the noise figure and conversion loss are acceptable at about 6 dB. The LO rejection is roughly 25 dB, and depends mainly on the construction. The mixer is suitable for RF and IF signals up to 30 and 50 MHz respectively.

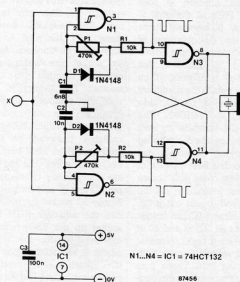
Piezoelectric resonators, also referred to as *buzzers*, are frequently used for providing audible signals in all sorts of electronic equipment. Buzzers are small, light, simple to use, and yet provide a loud output signal. They are either of the passive or of the active type. The former are driven by an AF signal source, while the latter feature a built-in oscillator, and require a direct voltage only.

This circuit is a double AF oscillator for driving passive buzzers. It ensures a richer output sound than normally obtainable from a piezo buzzer due to the use of two oscillators,  $N_1$  and  $N_2$ , whose output signal lies between 1 and 10 kHz. Gates  $N_3$ - $N_4$  form an S-R bistable which is controlled by the outputs of  $N_1$ - $N_2$ , and drives the buzzer direct. The spectral composition of the output signal is fairly complex, due to

the presence of both the fundamental notes and the difference and sum frequency. The timbre so obtained varies as a function of the ratio between the oscillator frequencies, which are adjustable with the aid of presets  $P_1$ - $P_2$ . Note that diodes  $D_1$ - $D_2$  reduce the duty factor of the oscillator signals to about 25%. Optimum effects are achieved when a simple ratio is set between the oscillator frequencies, e.g. 3:4. The resulting waveform is always composed of rectangular signals, but these differ in respect of their period to ensure that the buzzer produces a rather agreeable sound.

The buzzer driver is controlled by a logic level applied to point X. The quiescent current consumption is virtually negligible, while about 10 mA is drawn in the actuated state.

D



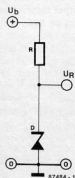
It is generally known that the accuracy of measurements in electronic circuits is mainly a function of the stability and reliability of the reference against which the unknown quantity is compared. Therefore, everything feasible should be done to maintain the stability of the reference, i.e., counteract

the adverse effects of variations in the ambient temperature, supply voltage, and load current. The zener diode in Fig. 1 is a usable reference device for applications where the above three parameters are not subject to appreciable variation. The "super zener" in Fig. 2 features excellent stability and

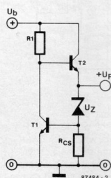
is hardly affected by variations in the supply voltage and the load current. Although the temperature coefficient of the super zener circuit can be optimized by careful dimensioning of the components, there exists a still better way for making a precision voltage reference.

The term *band gap* refers to the difference between two discrete energies of the outer four electrons in a semiconductor atom. Electrons in the highest energy band contribute to the conduction of the material. As the temperature is increased, some electrons gain enough thermal energy to escape from

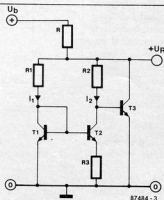
1



2



3



the valence (non-conductive) band, cross the band gap, and enter the conduction band, leaving the valence band unfilled. Thus, conductivity is a function of temperature.

With reference to Fig. 3, the temperature coefficient of current mirror  $T_1$ - $T_2$  is compensated by that of  $T_3$ . The following conditions should be met if the circuit is to function optimally: (1)  $R_2 = 10R_1$ ; (2)  $R_3$  is dimensioned such that  $V_R = 1.204$  V; and (3) the transistors are exactly matched. The latter condition is probably best satisfied by using transistors on one and the same chip carrier, e.g. those in a transistor array such as the Type CA3083. The value of  $R$  de-

pends on the supply voltage and the maximum output current. It should be noted that  $T_3$  carries the output current if the circuit is not loaded, so that the resulting dissipation may give rise to temperature differences on the chip. It is, therefore, recommended to permanently load the band-gap reference. The accompanying calculations prove that the output voltage of the circuit is not affected by temperature variations.

SV

#### Band-gap reference.

The reference voltage,  $U_R$ , is obtained from

$$U_R = U_{BE12} + I_R T_2$$

$R_1$  and  $R_2$  are dimensioned such that  $I_R = 10I_2$ , so that  $R_2$  drops  $[U_{BE11} - U_{BE12}]$  volts.

When the current amplification of  $T_2$  is sufficiently high,  $R_3$  carries virtually all current  $I_2$ :

$$I_2 = U_{BE11} - U_{BE12} / R_3 \text{ whence}$$

$$U_R = U_{BE12} + (U_{BE11} - U_{BE12}) R_2 / R_3$$

For identical transistors  $U_R$  is given for different values of  $I_2$  as

$$U_{BE11} - U_{BE12} = A T_2 / \log(d_1 / d_2)$$

$U_R$  of  $T_3$  is also expressed as

$$U_{BE13} = U_{BE11} - T_1 / T_2 + U_{BE11} / T_2$$

so that  $U_R$  can be written as

$$U_R = U_{BE11} - T_1 / T_2 + U_{BE11} / T_2 + R_2 / R_3 T_2 / \log(d_1 / d_2)$$

Differentiating this to the temperature domain yields

$$dU_R / dT = - U_{BE11} / T^2 + U_{BE11} / T^2 + R_2 / R_3 A / \log(d_1 / d_2)$$

If  $R_2$ ,  $R_3$  and  $I_R$  are dimensioned such that

$$R_2 / R_3 A \log(d_1 / d_2) = I_R U_R - U_{BE13} / T^2$$

where  $C = q / k T$

which results in

$$dU_R / dT = 0 \text{ (OED).}$$

$k$  = Boltzmann's constant ( $1.3805 \times 10^{-23}$  J/K).

$T$  = absolute temperature [K].

$q$  = charge of an electron ( $1.6021 \times 10^{-19}$  C).

$U_{BE}$  = band-gap potential (1.204 V).

$U_{BE0}$  = base-emitter voltage at  $T = T_0$ .

$e$  = the base of natural logarithms (2.71828).

## 24

# CURRENT MONITOR AND ALARM

by R Kambach

These circuits are intended for remote monitoring of the current consumption on the domestic mains line.

The circuit in Fig. 1 lights the signal lamp upon detecting a mains current consumption of more than 5 mA, and handles currents of several amperes with appropriate diodes fitted in the  $D_1$  and  $D_2$  positions. Transistor  $T_1$  is switched on when the drop across  $D_1$ - $D_2$  exceeds a certain level. Diodes from the well-known IN400x series can be used for currents of up to 1 A, while IN540x types are rated for up to 3 A. Fuse  $F_1$  should, of course, be dimensioned to suit the particular application.

A number of possible transistor types have been stated for use in the  $T_1$  position. Should you consider using a type not listed, be sure that it can cope with surges up to 700 V. As long as  $T_1$  does not conduct, the gate of the triac is at mains potential via  $C_1$ , protective resistor  $R_2$  and diode  $D_3$ , which keeps  $C_1$  charged. When  $T_1$  conducts, alternating current can flow through the capacitor, and the triac is triggered, so that  $La_1$  lights.

The circuit in Fig. 2 is a current triggered alarm. Rectifier

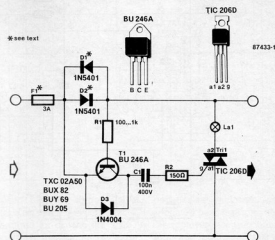
bridge  $D_4$ - $D_7$  can only provide the coil voltage for  $Re_1$  when the current through  $D_1$ - $D_2$  exceeds a certain level, because then series capacitor  $C_1$  passes the alternating mains current. Capacitor  $C_1$  may need to be dimensioned otherwise than shown to suit the sensitivity of the relay coil. This is readily effected by connecting capacitors in parallel until the coil voltage is high enough for the relay to operate reliably.

W

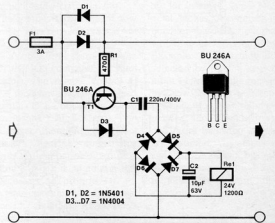
Finally, an important point:

**Many points in these circuits are at mains potential and therefore extremely dangerous to touch.**

1



2



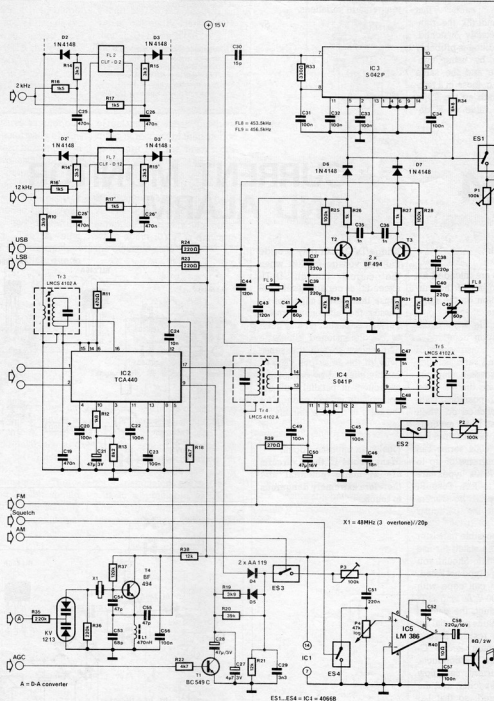
The intermediate frequency (IF) module shown in Fig. 1 accepts 48 MHz, and is suitable for receiving AM, FM and SSB transmissions. CW reception

should also be possible in the SSB mode when a sufficiently narrow bandfilter is included ( $BW < 500$  Hz). For radioteletype (RTTY), it is best to

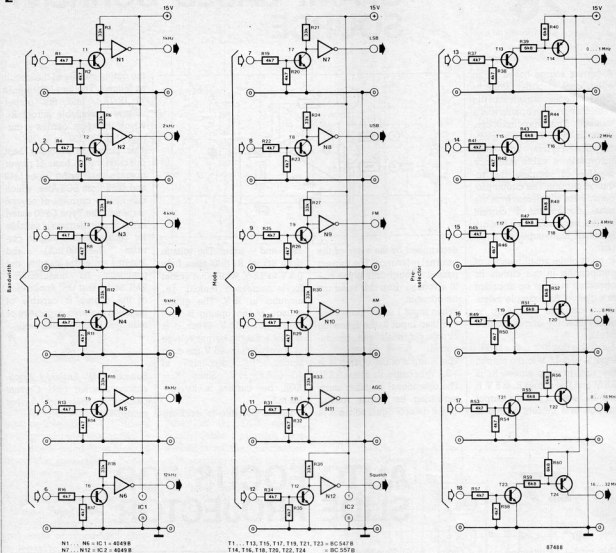
drive a comparator from the FM detector output.

There is no need for a high level mixer to convert the input down to 455 kHz, since the 48 MHz

signal has already been filtered and occupies a bandwidth of only 12 kHz. The RF and mixer stages in the TCA440 operate up to 50 MHz, while the built-in







AGC has a dynamic range of about 100 dB. The mixer output is fed to diode switches to enable digital selection of the appropriate bandwidth.

The proposed selection circuit ensures a filter separation of the order of 80 dB. The choice of the 455 kHz filters is governed by the particular application and the financial means available. The CLF-D12 and CLF-D2 are for FM/AM and SSB respectively; the number in the type indication stands for the bandwidth. The Type CLF-D4 or CLF-D6 can be used equally well for communication quality AM. Unfortunately, narrow-band filters for CW and RTTY are difficult to obtain, but "add-on" 500 Hz or 250 Hz filters for commercially available receivers and transceivers (Yeasu,

Kenwood) can be used here with excellent results.

The IF output from IC<sub>1</sub> is rectified for the AM and AGC sections, and inductively fed to FM detector IC<sub>2</sub> as well as to product detector IC<sub>3</sub>. Note that in general no AGC action is required in the FM and RTTY mode. The BFO for the product detector is based on USB and LSB ceramic resonators, which are found in most SW receivers of far Eastern origin, but may be difficult to obtain as a one off. The circuit around T<sub>4</sub> is a voltage-controlled 48 MHz crystal oscillator (VCXO) that operates in the parallel mode, requiring due attention to be paid to the correct output frequency if a common, series-resonant crystal is used. The synthesizer for tuning the pro-

posed receiver outputs 1 kHz steps, so that a D-A converter is required for driving the VCXO input. A resolution of 10 Hz should be adequate to ensure smooth and reliable tuning.

The computer interface for controlling the receiver is shown in Fig. 2. This is essentially a 5 V to 15 V logic level converter with TTL/CMOS compatible control inputs. The remote control of the receiver obviates the need for this to be housed in a neat enclosure. Albeit that the receiver features need not have a "desktop" appearance with all the controls fitted on a front panel, it is, of course, still necessary to provide for adequate screening and thermal stability. Sufficient AF power is available from IC<sub>3</sub> to drive a relatively long cable to the

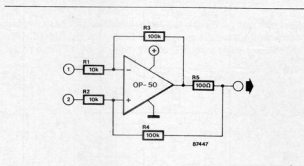
loudspeaker enclosure, which is located near the computer. The receiver can be controlled from any computer that has three 8-bit output ports based on, for instance, Type 74LS374 octal latches. A receiver function is enabled when a logic 1 is written to the respective input. Example: 4 kHz bandwidth is selected by driving BANDWIDTH input 4 high, and the remaining five low. Writing a computer program for controlling the receiver should not be too difficult if the following sequence is observed: 1. actuate the squelch; 2. reset all bits on the relevant control port; 3. set the required bit; 4. turn off the squelch.

B

A current source based on an operational amplifier alone is likely to be less known than the combination of an opamp and a transistor. This latter circuit can, however, only supply a unidirectional current, and must incorporate a stable reference capable of sourcing the required current. The circuit proposed here is different from the usual design for a current source, because it has a real differential, high impedance, input.

In spite of the small number of components in this circuit, its operation may not be apparent at a glance. An example calculation example may help to clarify how the current source works.

Assuming that 10 V is applied to input 2, and 4.5 V to the output, the voltage drop across  $R_2$  is 0.5 V, and that across  $R_4$  is 5 V. It will be recalled that the output voltage of a current source is



determined by the value of the external resistance. The current passed through this gives rise to a voltage drop that need not be constant.

When input 1 is 1 V more positive than input 2, the following circuit potentials can be deduced:

The + input of the opamp is at +9.5 V, because  $R_2$  drops 0.5 V. The operational amplifier starts regulating its output voltage until it detects equal voltages at

its + and - input. The voltage drop across  $R_1$  thus rises from 0.5 V to 1.5 V, while that across  $R_3$  is increased tenfold, i.e., amounts to 15 V. The output voltage of the opamp is then  $11 - 1.5 - 15 = -5.5$  V. When it is recalled that the output voltage of the circuit is +4.5 V, the drop across  $R_5$  amounts to  $4.5 - (-5.5) = 10$  V. Since  $R_5 = 100\Omega$ , the current is  $10/100 = 100$  mA.

It is also possible to establish

the output current of the circuit as follows. The amplification is  $10 (R_3/R_1)$ , and the output voltage is available across  $R_5$ , which therefore carries a current of  $U_i \times 10/100$ , or  $U_i/10$ . This circuit is probably best operated on the basis of power opamps, such as the Types LI49 and LI50 from SGS-Ates, which can handle currents of several amperes. The Type OP50 stated in the circuit diagram is suitable for relatively low output currents ( $I_{max} = 50$  mA), and features excellent stability and precision. Its manufacturer, PMI, states that this application of the opamp is capable of handling resistive, capacitive or inductive loads equally well.

W

Source: PMI, Analog Applications Seminar 1986: Current transmitter (Howland current pump).

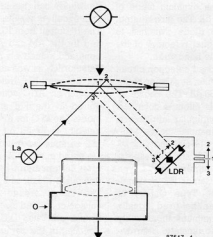
This circuit is intended as a replacement for the electronics in a partly or wholly defective autofocus driver in a slide projector. The mechanical parts in the autofocus system are assumed to be still functional.

Most automatic focusing systems in slide projectors are based on the use of an optical module, which comprises a small lamp, a few lenses and mirrors, and a light sensor made from two series-connected light dependent resistors (LDRs), which function as a potential divider. As shown in Fig. 1, lamp  $L_a$  projects a narrow beam onto the centre of the slide, A, whose surface reflects it onto the LDRs. When the slide surface bulges inside or outside, the projected image on the screen is blurred, and the beam from  $L$  is received on the surface of one of the LDRs

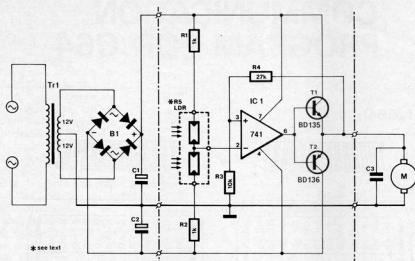
(point 2 or 3). This is detected by a motor driver circuit, which ensures that the focal distance between the objective, O, and the slide surface is corrected to maintain a sharp image, i.e., the objective is moved until the circuit detects that the reflected beam from L falls exactly in between the LDRs (point 1).

The circuit is based on the use of an existing set of LDRs as part of the optical module in the slide projector. The symmetrical supply shown to the left, and the motor plus decoupling capacitor, are also part of the projector. The inverting input of opamp IC1 is at ground potential when the above mentioned test beam falls in between the LDRs. The output of the opamp keeps the non-inverting input at 0 V as well, so that no motor voltage is available at the emitters of power drivers  $T_1$ - $T_2$ .

1



87517-1



Should the reflected beam illuminate either one of the LDRs, the circuit arranges for the motor to move the objective glass towards the correct focal position, until no voltage difference between the LDRs is detected.

The feedback gain of the circuit has been kept relatively low to keep the motor from continuously moving the objective glass past the target position, causing the system to oscillate slowly. Resistors  $R_3$  and  $R_4$  may have to be dimensioned differently than shown to achieve optimum response as regards speed and stability.

R

## 28

## DRIVE SELECTOR

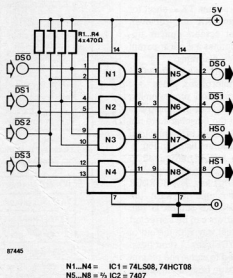
This circuit makes it possible to use double-sided disk drives with a computer that supports only single-sided units. Many of the older generation of computers were designed to operate in conjunction with Shugart-compatible, single-sided disk drives. These have rapidly been superseded, however, by the more economical double-sided drive, which has a greater storage capacity.

The Shugart standard supports the use of four disk drives, which are selected with drive select lines DS0-DS3. Two further lines, HS0 and HS1, control the head selection on each of these drives. When this circuit is installed between the computer's disk controller output and two double-sided drives, the disk operating system (DOS) can recognize four logical drives. When the computer selects drive A or B, the situation is similar to before the conversion. Selection of drive C or D, however, causes the second head in the relevant drive A or B to be activated. In this way, the total storage capacity of the double-sided drives is available even under "primitive" circumstances.

Note that the use of drive denotations A-B-C-D or 0-1-2-3 is

particular to the type of computer, or the DOS version. Finally, Table 1 provides information about the combination of the original four DS lines into two HS and two DS lines.

D



87445

N1...N4 = IC1 = 74LS08, 74HCT08  
N5...N8 = IC2 = 74157

Table 1

logical drive	DS3 DS2 DS1 DS0					DS0 DS1 HS0 HS1					physical drive	
A (1)	=	1	1	1	0	→	0	1	0	1	=	A side 0
B (2)	=	1	1	0	1	→	1	0	0	1	=	B side 0
C (3)	=	1	0	1	1	→	0	1	1	0	=	A side 1
D (4)	=	0	1	1	1	→	1	0	1	0	=	B side 1

This program enables users of the popular Commodore C64 home computer to exchange messages between two machines.

No hardware whatsoever is needed to accomplish:

- communication over several tens of metres using a three-wire connection—see Fig. 1. Longer distances, or communication over the telephone, of course require the use of a modem.
- split screen operation: the upper half of the screen displays the operator's input (LOCAL), the lower half displays the received messages (REMOTE).
- full duplex communication, i.e. transmission and reception are quasi-simultaneous processes.

The flowcharts in Fig. 2 illustrate the structure of the proposed program. **TX** is short for transmitter, **RX** for receiver. Note that screen pointer updating routines are not apparent from these diagrams.

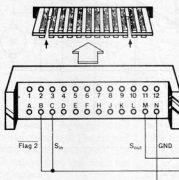
Unfortunately, since the C64 BASIC interpreter does not allow structured programming to be carried out, the constructs shown in the flowcharts are not readily detected in the practical BASIC program listed in Fig. 3. Keyed-in text is transmitted to the far computer after pressing the RETURN key. The BORDER colour changes to warn the user when the screen is full. Typing errors can be corrected in the usual way with the aid of the INST/DEL key. A short beep is sounded to signal the receipt of a message from the REMOTE computer.

Testing the program is straightforward, and does not require two computers. Figure 4 shows the connections that can be made temporarily on the computer's user port. This creates a zero modem, and causes LOCAL text to be echoed on the REMOTE screen.

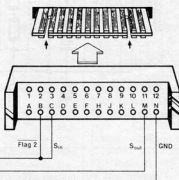
For those computer enthusiasts interested in analysing the BASIC program, and for those who intend to rewrite it for

1

I (C64):

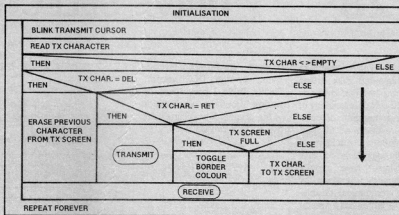


II:

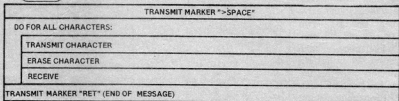


2

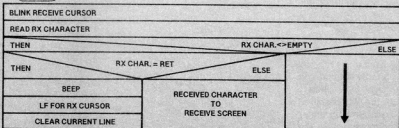
\* MAIN LOOP



\* TRANSMIT SUBROUTINE



\* RECEIVE SUBROUTINE



other types of computer, the function of the major lines can be summarized as follows:

**100-125:** initialize the screen and the sound generator.

**130:** open the serial port with parameters 300 baud, 8 data bits, 1 stop bit, no parity, no handshaking, full duplex.

**140:** T is the base address of the transmit screen, and T0 is the associated index. R and R0 are similar variables for the receive screen, while R1 in addition gives the maximum number of character per line.

**160:** blink the cursor and read the keyboard buffer.

**180-200:** test for DELETE, and erase the previous character.

**210-230:** test for RETURN and transmit message.

**240-260:** toggle the BORDER colour when the screen is full.

**270:** go to the receive sub-routine.

**280:** repeat the above loop.

**710:** transmit the "begin of message" marker.

**720-750:** transmit and erase all characters. Monitor the receive channel for messages, after transmission of every character, reception has the highest priority.

**760:** transmit the "end of message" marker.

**810:** blink the cursor and read the receive buffer.

**820:** buffer empty?

**830:** end of message.

**840:** have the sound generator produce a beep.

**850-870:** advance the cursor to the next line.

**880:** clear the new line.

**900:** display received character on REMOTE screen.

**910-920:** advance cursor to next position.

W

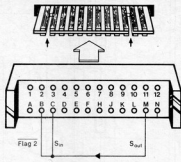
3

```
100 POKES3261.12:PRINT"":POKES3260.9:POKES3261.0:PRINT CHR$(152):POKES3272.23
110 S1=54272:POKE 24+S1.15:POKE S1.207:POKE 1+S1.34:POKE 5+S1.18
120 FOR H=1833 TO 1844: READ A: POKE H,A: NEXT H
125 FOR H=1273 TO 1283: READ A: POKE H,A: NEXT H
130 OPEN 2,2,0,CHR$(6)+CHR$(0)
140 T=1104: T0=0: R=1344: R0=0: R1=0
150 REM MAIN
160 POKE T+T0.60: POKE T+T0.32: GET T$
170 IF T$="" THEN GOTO 270
180 IF T$<>CHR$(20) THEN GOTO 210
190 IF T0=0 THEN T0=T0-1
200 POKE T+T0.32: GOTO 270
210 IF T$<>CHR$(13) THEN GOTO 240
220 GOSUB 700
230 GOTO 270
240 IF T+T0=R-80 THEN GOTO 260
250 POKE T+T0.ASC(T$): T0=T0+1: GOTO 270
260 POKE 53260.1: FOR H=0 TO 15: NEXT H: POKE 53260.9
270 GOSUB 800
280 GOTO 150
700 REM TRANSMIT
710 PRINT#2,CHR$(62): PRINT#2,CHR$(32):
720 FOR K=T TO T+T0-1
730 PRINT#2,CHR$(PEEK(K)): POKE K,32
740 GOSUB 800
750 NEXT K
760 PRINT#2,CHR$(13): T0=0
770 RETURN
800 REM RECEIVE
810 POKE R+R0.60: POKE R+R0.32: GET#2,R$
820 IF R$="" THEN GOTO 930
830 IF R$<>CHR$(13) THEN GOTO 900
840 POKE 54276.0: POKE 54276.33
850 IF R1=40 OR R1=0 THEN GOTO 870
860 POKE R+R0.32: R1=R1+1: R0=R0+1: GOTO 850
870 R1=0: IF R+R0=2024 THEN R0=0
880 FOR H=R+R0 TO R+R0+39: POKE H,32: NEXT H
890 GOTO 930
900 POKE R+R0.ASC(R$): R0=R0+1: R1=R1+1
910 IF R1=40 THEN R1=0
920 IF R+R0=2024 THEN R0=0
930 RETURN
950 DATA 42,32,84,82,65,78,83,77,73,84,32,42
960 DATA 42,32,82,69,67,69,73,86,69,32,42
970 END
```

READY.

4

C64:



30

## FLASHING REAR LIGHT

by J Donhauser

This rear light for bicycles is fed from a battery charged with current from the dynamo, and starts to flash when the cyclist halts. To preserve battery power, the unit automatically switches off 4 minutes after halting.

The circuit is essentially composed of a battery charger and a logic switching section. The NiCd battery is charged from a voltage doubler C<sub>1</sub>-C<sub>2</sub>-D<sub>1</sub>-D<sub>2</sub>-C<sub>3</sub> to ensure a charge current of about 20 mA when riding at a reasonable speed. This makes it possible for a charge of 3 mAh to be available after a 10

minute ride, i.e., enough for the light to flash for about 4 minutes after the bicycle is halted. A relay is used to switch between operation while riding and while standing still. When the bicycle is in motion, the voltage from the dynamo, G, ensures that N<sub>1</sub> is enabled, so that T<sub>1</sub> actuates Re, and the small 6 V

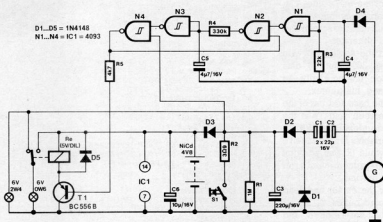
bulb is illuminated. Since C<sub>2</sub> is only slowly discharged via R<sub>1</sub>, N<sub>1</sub> remains enabled for about 4 minutes after halting. Push-button S<sub>1</sub> enables immediately switching off the rear light, because R<sub>2</sub> then discharges C<sub>1</sub> in a few seconds.

Gate N<sub>1</sub> monitors the dynamo voltage, which is rectified by

D4-C4-R3. When the current voltage drops below approximately 2 V, N1 switches on multivibrator N2-N3-N4 which causes the relay to toggle at a rate determined by R4-C5. The 5 V DIL relay requires only 11 mA, while the current consumption of the 4093 is virtually negligible at about 1  $\mu$ A.

It should be possible to fit the circuit and the battery in a somewhat larger than normal bicycle headlight, equipped with terminals for connecting the dynamo and the rear light. Of course, due care must be taken to avoid the battery contacts touching the metal inside of the light.

R



87446

## 31

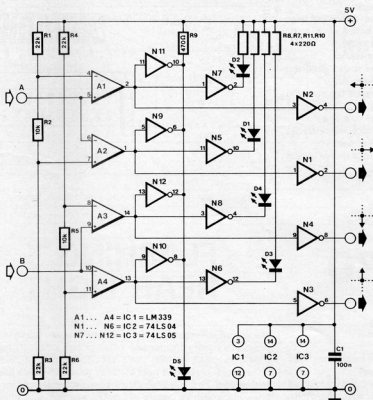
## A-D CONVERTER FOR JOYSTICKS

From an idea by F Berben

Although joysticks come in an astounding variety of versions, their internal organization is virtually always a standard concept, based on either a set of relatively fragile, springy, membrane contacts, or two potentiometers. Many computer enthusiasts will agree that the latter, analogue, type offers better reliability and quality. Unfortunately, however, these can not be used in conjunction with a popular home micro such as the Commodore C64, and that is where the present circuit comes in.

The four comparators in IC1 function as switches to translate the handle movement into digital signals. The outputs of the comparators are buffered in IC2 to enable interfacing to the computer's joystick port. The two remaining inverters in IC2, N5 and N6, along with two inverters in IC3 function as drivers for the LEDs that indicate the handle position. Gates N7-N12 are set up as a wired NOR function to enable LED D5 to light when the joystick handle is in the centre position. Finally, the current consumption of the converter is about 25 mA.

D



87417

Many of today's HiFi amplifiers feature a "clicking" volume control, but this is only rarely a real stepped attenuator based on a wafer switch. In nearly all cases, this expensive system is based on a normal potentiometer, whose spindle is fitted with a mechanical construction to simulate the stepping movement. A normal rotary switch is not suitable for adjusting the volume of an amplifier because it briefly disconnects the input from the signal source when operated, and so readily gives rise to clicks and contact noise. Different problems crop up when designing an electronic volume control. Of these, distortion is probably the hardest to master, but reasonable results are still obtainable, as will be shown here.

Basically, there are two methods for making an electronic potentiometer. One is to create a tapped resistor ladder (which is not much different from a normal potentiometer), the other is to change the resistance of the two "track sections" such that the total resistance remains constant. The circuit proposed here is based on the second method, and features 16 steps in its basic form. The number of steps can be increased to, say, 64 by adding four switches and resistors.

The electronic potentiometer is composed to two equal sections, which have a total resistance of 15 k $\Omega$  each. The electronic switches in each section are controlled by binary counter ICs. Since the switches in section ES<sub>1</sub>-ES<sub>4</sub> and those in ES<sub>5</sub>-ES<sub>8</sub> are controlled in complementary fashion, the total resistance of the potentiometer remains constant. Resistors R<sub>1</sub>-R<sub>4</sub> and R<sub>7</sub>-R<sub>8</sub> serve to keep the potential at the input and output at 0 V so as to preclude clicks when the step switch, S<sub>2</sub>, is operated. Switch S<sub>1</sub> is the up/down selector. Gates N<sub>5</sub>-N<sub>6</sub> form a bistable to ensure that the counter is clocked with debounced step pulses.

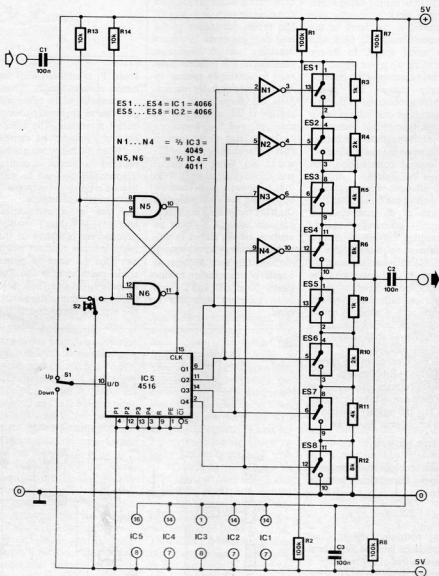
The number of steps can be increased by adding a counter and the required number of electronic switches, divided

over the two "track sections". These switches are then connected in parallel with resistors whose values correspond to binary order 1-2-4-8, etc., as

shown in the circuit diagram. Fortunately, precise binary ratios are not required here, since adequate results are obtainable with approximations

of the theoretical resistance values, and as long as the actual resistors are kept equal in both sections.

D



87401

Simple DC operated motors with a permanent magnetic stator behave as an independently energized motor. The speed of an ideal motor with an infinitely low internal resistance is in direct proportion to the voltage applied, irrespective of the torque. The motor thus runs at a speed at which its reverse electromotive force (e.m.f.) equals the supply voltage. The reverse e.m.f. is directly proportional to the force of the (constant) magnetic field, and the motor speed. In theory, therefore, the motor speed can be held constant with a constant supply voltage. The speed reduction observed in practice arises from the voltage drop across the internal resistance,  $R_i$ , of the armature winding. Thus, when the motor is loaded, its current consumption, and hence  $V_{R_i}$ , increases, reducing the effective supply voltage. This effect can be eliminated by means of  $R_i$  compensation, which essentially entails measuring the motor's current consumption, relating this to the motor's instantaneous drop across  $R_i$ , and increasing the supply voltage accordingly. In fact, this calls for a voltage source with a negative output impedance, since it caters for a higher output voltage when the load is increased.

The basic set-up of the supply required here is shown in Fig. 1. The load current is measured as the drop across sensing resistor  $R_s$ . The DC transfer function of this amplifier is written as

$$U_2 = U_1 + I_L R_s R_3 / R_1$$

which accounts for the negative output impedance because then

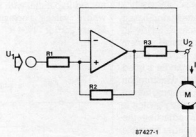
$$R_{out} = -R_s R_3 / R_1$$

For optimum results, this impedance must be kept about equal to that of the motor.

Figure 2 shows the practical circuit of the motor driver based on a power operational amplifier. The Type L165 from SGS can supply up to 3 A at a maximum supply voltage of 36 V, and is therefore eminently suitable for the present appli-

cation. Capacitors  $C_1$  and  $C_2$  suppress noise on the reverse e.m.f. from the motor. Due care should be taken, however, in so extending the circuit, because this readily leads to instability. The motor itself already forms a fairly complex load, since the revolving rotor winding is mainly inductive, and the rotor itself represents a fairly large capacitance. Noise suppression components such as  $R_4$  and  $C_3$  add to the complexity of the load and may result in control instability, which becomes manifest in the motor's tendency to alternately reverse its direction at a relatively low rate. Also, the response to a fast change in the torque may be impaired, and high-frequency oscillation may occur (noticeable as excessive heating of  $IC_1$  and/or  $R_4$ ). When the circuit was tested with a small PCB drill, best results were obtained by omitting  $R_4$ - $C_3$  and including  $C_2$ . If the motor has a noise suppression network,  $C_2$  must be omitted, and  $R_4$  added to protect the opamp inputs against too high differential voltages as a result of commutation voltage peaks. Clearly,  $D_1$  and  $D_2$  have been included with this in mind.

1



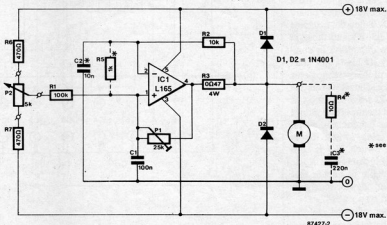
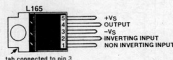
87427-1

Preset  $P_1$  is adjusted until the motor remains stable. Overcompensation of the motor will give rise to apparently uncontrolled movement. The adjustment of  $P_1$  should be carried out when the motor has not yet reached its normal operating temperature, because its self-heating gives rise to an increase in the internal resistance. The use of a symmetrical supply ( $\pm 18$  V max.) enables two-quadrant operation of the motor (cw/ccw rotation), which can then be used to power model trains and the like. The motor is halted when  $P_2$  is set to the centre position. The ground rail may be connected to the

negative supply rail if only one direction of revolution is required (PCB drills). The maximum supply is then 36 V, making a greater voltage available for the motor, so that 24 V types can be controlled also, although it is not possible to completely halt these.

The motor can be protected against overloading by selecting a supply voltage that causes the opamp to clip when it outputs the maximum motor current. Finally,  $IC_1$  is capable of supplying considerable current, and must, therefore, be fitted with a fairly large heat-sink. The quiescent current of the circuit is about 50 mA. TW

2



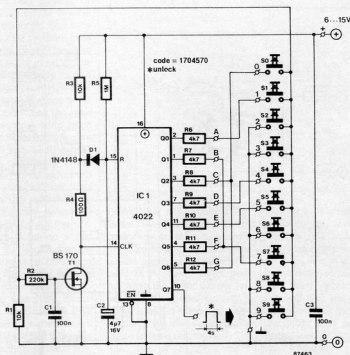
87427-2





This code lock provides a high degree of security whilst being a very simple design. At the heart of the circuit is the Type 4022 octal counter. In the non-active state,  $C_2$  is charged via  $R_5$ , so that the reset (R) input of the counter is kept logic high. This causes output  $Q_0$  to be actuated, while all other outputs are logic low. When  $S_1$  is pressed,  $T_1$  is switched on via debouncing network  $R_2-C_1$ , and  $IC_1$  receives a clock pulse. Also,  $C_2$  is discharged via  $R_4-D_1$ , ending the reset state of the counter and enabling it to advance. The time required for  $R_5$  to recharge  $C_2$ , i.e., to reset the counter, is the maximum time that can lapse before the next key is pressed. The above cycle is therefore repeated only when  $S_7$  at the  $Q_7$  output is pressed in time and in the correct order,  $Q_7$  goes high for about 4 seconds to enable driving the unlock circuitry, e.g. a relay driver for an automatic door opener. The code for the lock shown in the circuit diagram is 1704570: this is but an example, however, and the combination code is readily altered by swapping connec-

1

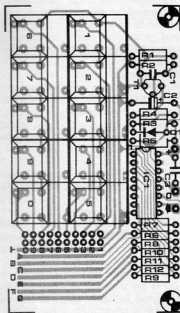
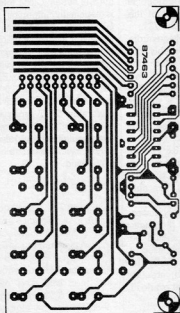


tions between the counter outputs and the switches. When the 7-digit code is considered too simple to crack, the 4022 can be replaced by a 4017,

which makes it possible to add two keys. This means that the number of combinations is  $10^9$  instead of  $10^7$ . The quiescent current con-

sumption of the code lock is negligible at  $0.5 \mu A$ , so that battery operation is feasible. The circuit works well from any supply between 6 and 15 V.

2



#### Parts list

##### Resistors ( $\pm 5\%$ ):

- $R_1, R_3 = 10K$
- $R_2 = 220K$
- $R_4 = 100R$
- $R_5 = 1M\Omega$
- $R_6 \dots R_{12}$  incl. =  $4K7$

##### Capacitors:

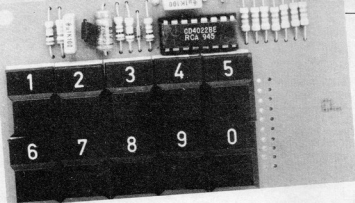
- $C_1, C_2 = 100n$
- $C_2 = 4\mu F; 16V$ ; axial

##### Semiconductors:

- $D_1 = 1N4148$
- $IC_1 = 4022$
- $T_1 = BS170$

##### Miscellaneous:

- $S_6 \dots S_9$  incl. = Digitast momentary action button (SE or S version, ITT Schadowl).
- PCB Type 87463 (not available through the Readers Services)



The accompanying photograph shows that the code lock can be built as a very compact unit thanks to the use of a printed circuit board that holds the 10 keys also.

Sv

## 36

## THERMOMETER

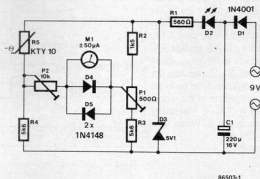
from an idea by P Needham

At the heart of this simple circuit is the well-known Type KTY10 temperature sensor from Siemens. This silicon sensor is essentially a temperature-dependent resistor, which is connected as one arm in a bridge circuit here. Preset  $P_1$  functions to balance the bridge at  $0^\circ\text{C}$ . At that temperature, moving coil meter  $M_1$  should not deflect, i.e., the needle is in the centre position. Temperature variations cause the bridge to be unbalanced, and hence pro-

duce a proportional indication on the meter. Calibration at, say,  $20^\circ\text{C}$  is carried out with the aid of  $P_2$ .

The bridge is fed from a stabilized 5.1 V supply, based on a temperature-compensated zenerdiode. It is also possible to feed the thermometer from a 9 V battery, provided  $D_1$ ,  $R_1$  and  $C_1$  are replaced with a Type 78L05 voltage regulator, because this is more economic as regards current consumption.

TW

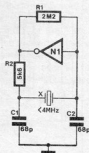


## 37

## PIERCE OSCILLATOR

In addition to the description elsewhere in this magazine of HC and HCT based R-C/L-C oscillators for use up to 20 MHz, this design brief concentrates on quartz-controlled oscillators which find applications in digital equipment and micro-processor systems. Such oscillators can only be made with HCU gates, because HC and HCT ones have buffered outputs that make them unsuitable for use as analogue amplifiers.

The circuit diagram shows a Pierce oscillator set up around a single gate in a Type



$N1 = 1/6 \text{ IC1} = 74\text{HCU04}$   
67407



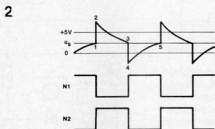
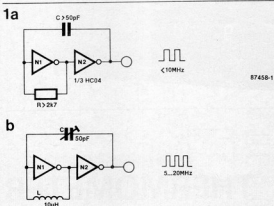
74HCU04 package. The inverter functions as an inverting amplifier with a phase shift of  $180^\circ$ . The circuit can be modified into a Colpitts oscillator by replacing the quartz crystal with an inductor. It should be noted, however, that the use of a quartz crystal is more appropriate because it ensures minimum current consumption and adequate suppression of the third harmonic frequency. Finally,  $R_2$  must be replaced with a 33pF capacitor if the oscillator is operated above 4 MHz.

Sv

Two inverters, one resistor and one capacitor are all that is required to make a HC(T)-based oscillator that gives reliable operation up to about 10 MHz. This sort of circuit is well-known, and appears in Fig. 1a.

The use of two HC inverters gives fairly good symmetry of the rectangular output signal. In the same circuit, HCT inverters give a duty factor of about 25%, rather than about 50%, since the toggle point of an HC and an HCT inverter is  $\frac{1}{2}V_{cc}$ , and slightly less than 2 V, respectively.

When the supply voltage for the oscillator is switched on, C is initially has no charge, and the output of  $N_1$  and  $N_2$  are at the same logic level. Capacitor C is then charged via R, until it has acquired a charge voltage that corresponds to the toggle voltage,  $U_{th}$ , of  $N_1$ . Assuming the output of  $N_2$  initially to be logic low, the waveform of the signal at the input of  $N_1$  is essentially as shown in Fig. 2. When C is



charged up to level 1, the output of  $N_1$  toggles, and so does that of  $N_2$ . This causes the voltage at the input of  $N_1$  to rise, via C, to about  $1.5V_{cc}$ , so that C is reverse charged to level 3. From there on, the amplitude changes in a mirror-inverted way to reach the initial state again (level 5 is identical to 1), and the circuit oscillates. In practice, the curve in Fig. 2 is slightly flatter, because the peaks at levels 2 and 4 are clamped to +5 V and 0 V by the protective circuits internal to the inverters.

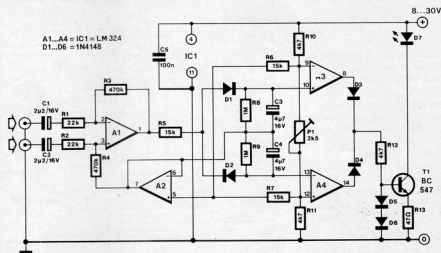
If the oscillator is to operate above 10 MHz, the resistor is replaced with a small inductor, as shown in Fig. 1b.

The output frequency of the circuit in Fig. 1a is given as about  $1/18RC$ , and can be made variable by connecting a 100K preset in series with R. The solution adopted for the oscillator in Fig. 1b is even simpler: C is a 50 pF trimmer capacitor.

D

On most FM tuners, the stereo indicator lights upon detection of the 19 kHz pilot tone. However, this need not mean that the programme is actually stereophonic, since the pilot tone is often transmitted with mono programmes also. A similar situation exists on stereo amplifiers, where the stereo LED is simply controlled from the mono-stereo switch.

The LED-based stereo indicator described here lights only when a true stereo signal is fed to the inputs. Differential amplifier  $A_1$  raises the difference between the L and R input signals. When these are equal, the output of  $A_1$  remains at the same potential as the output of  $A_2$ , which forms a virtual ground rail at half the supply voltage. When  $A_1$  detects a dif-



ference between the L and R input signals, it supplies a positive or negative voltage with respect to the virtual ground rail, and so causes  $C_2$  to be charged via  $D_1$ , or  $C_4$  via  $D_2$ . The resistors connected in parallel to these capacitors ensure slow discharging to bridge brief silent periods in the programme. Comparator A3-A4 switches on the LED driver via OR circuit D3-D4.

When building the circuit into an amplifier, care should be taken to select the right point from which the input signals are obtained. In general, this should be before the volume and balance controls, but behind the mono/stereo selector. The signal level should not be less than 100 mV to compensate for the drop across  $D_1$  or  $D_2$ . Also observe that the impedance at the selected

"tap" location is relatively low. Should the stereo light come on when a mono programme is being received, the input signals are different, and the sensitivity of one of the amplifier channels should be altered. If this is impossible or undesirable,  $R_3$  may be replaced by a series connected preset and a resistor. The sensitivity of the stereo indicator is adjustable with  $P_1$ . The current consump-

tion is less than 7 mA when the LED is off, and about 20 mA when it is on.

TW

## 40

# SYNCHRONIZATION SEPARATOR

from an idea by J W v Dijk

Many monitor chassis currently offered by computer surplus stores have separate inputs for horizontal and vertical synchronization signals. Most home micros, however, have a composite video output, so that some form of interfacing is required to drive these bargain monitors.

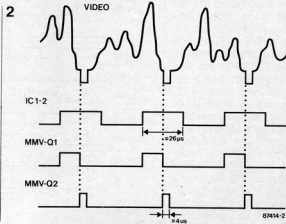
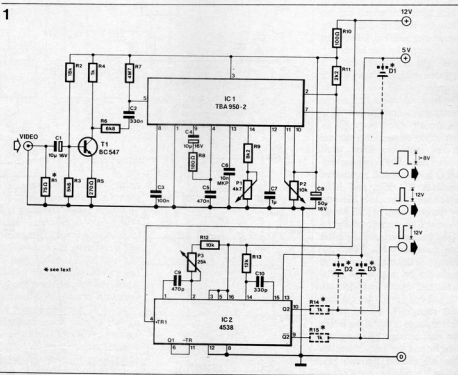
The Type TBA950-2 is a sync separator chip which is frequently encountered on TV chassis. In its standard application circuit, it requires to be driven by a flyback signal derived from the output of the line frequency oscillator. Without this signal, which is applied to pin 10, the sync pulse would end up somewhere among the picture lines. To be able to use the TBA950-2 in the present application, the horizontal pulse is slightly shifted with the aid of a double monostable multivibrator, IC2.

The operation of the circuit should be clear from the accompanying timing diagram. The output pulse from the TBA950 is fairly wide (26  $\mu$ s), and its positive edge triggers the first MMV (Q1), whose negative output pulse transition in turn triggers the second MMV in the 4538 package. The line sync pulse for the monitor is available positive and negative at IC2 outputs Q2 and Q2, respectively.

Adjust the circuit as follows: set  $P_2$  to the centre of its travel, and adjust the frequency control,  $P_1$ , such that the image is stable. Next, position the image by adjusting  $P_3$ . If the correct pos-

ition can not be obtained, the phase control,  $P_1$ , must be carefully readjusted, followed by  $P_3$ . The vertical sync pulse is available at pin 7 of the TBA950-2. Finally, the dashed resistors and diodes are required if the monitor inputs are designed to accept signals with a peak-to-peak amplitude of 5 V.

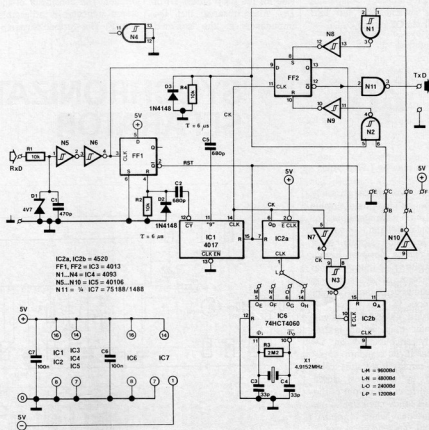
D



Some computers and communication programs are unable to output serial data composed of 7 data bits and a parity bit. The present circuit has been designed to output this data format when it is driven with serial data organized as 1 start bit, 8 data bits, no parity bit, and 1 stop bit. This format is widely used for accessing bulletin boards, data banks, and the like with the aid of a modem, and should be available on most computers equipped with an RS232 port. The converter has a built-in clock generator which can be set to the baud rates shown the circuit diagram, Fig. 1. Both odd and even parity can be generated, and no handshaking is required with the computer or console.

The basic operation of the converter is as follows (also refer to the timing diagram in Fig. 2). The rising edge of the start bit in the incoming 10-bit word clocks bistable FF<sub>1</sub>, whose output Q goes low and so enables counters IC<sub>1</sub>, IC<sub>2a</sub> and IC<sub>2b</sub>, which were previously blocked by the high level of RST. Binary counter IC<sub>2a</sub> starts counting the clock pulses provided by baud rate generator IC<sub>1</sub>. The frequency of this clock signal is 16 times the bit rate on the serial input and output line. Bistable FF<sub>2</sub> and counter IC<sub>1</sub> are clocked with signal CK, whose period corresponds to that of the bits in the data stream. The received start bit and the next seven data bits are passed through FF<sub>2</sub>, while IC<sub>1</sub> keeps count of the number of transmitted bits, and actuates output 9 during the reception of the ninth bit (i.e., databit 7). The rising edge of the counter output pulse is differentiated in C<sub>5</sub>-R<sub>5</sub> and then applied to NAND gates N<sub>1</sub>-N<sub>2</sub>. These make it possible for FF<sub>2</sub> to be set or reset, depending on the state of parity counter IC<sub>2b</sub>, which keeps count of the logic high bits in the serial word applied to the converter. Its output Q<sub>A</sub> indicates whether the number of detected high bits is odd (Q<sub>A</sub>=1) or even (Q<sub>A</sub>=0), and causes FF<sub>2</sub> to toggle when the differentiated pulse from IC<sub>1</sub> makes the output of N<sub>1</sub> or N<sub>2</sub>.

1



go high for a very short period. When  $Q_A$  is low, the parity bit at  $Q$  of  $FF_2$  is high because in that case the S (set) input is driven high. Similarly, the parity bit is low when  $Q_A$  is high because the R (reset) input on  $FF_2$  is then driven high. These two situations can occur when even parity is selected by fitting wire links A-D and B-C as shown in the circuit diagram. Odd parity is obtained by fitting links A-C and B-D, and permanently low parity by fitting C-E and D-F (note that a "low" parity level means that the relevant bit is logic high in the RS232 convention).

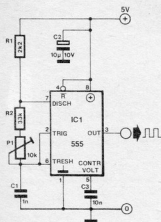
After transmission of the parity bit, the circuit is prepared for the next word by the carry (CY) output of  $IC_1$  providing a high

level to differentiator  $C_7$ - $R_4$ . This resets  $FF_1$ , which in response drives the RST line high to reset the counters.

The convention adopted for the logic high and low levels of the data bits in the proposed converter requires that this is inserted in an RS232 or RS432 data line. Line driver  $N_1$  may be omitted, and the serial output signal taken from  $Q$  on  $FF_2$ , if the driven input can operate with pulse levels of 0 and +5 V. Finally, Fig. 3 shows a suitable alternative for the crystal-operated clock generator, which may be considered too extensive if the circuit is to work at a fixed baudrate of 1200. Multi-turn preset  $P_1$  is set for an output frequency of 19,200 Hz.

Th

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87516-3

## 42

# TRANSMISSION LINES FOR TTL CIRCUITS

Although cable connections between TTL circuits are normally not as critical as those for, say, RF applications, it is still worth while to reflect on this subject because strange things often happen when a TTL transmission line is not correctly terminated. In particular, this discussion is about terminating coaxial cable and flat ribbon cable. The latter is frequently used for driving Centronics compatible inputs.

A commonly used coaxial cable is RG59B/U, which has a characteristic impedance of 75  $\Omega$  and a propagation delay of 5 ns/m. With signal rise and fall times of 4 ns, the cable may be considered electrically long if it exceeds 40 cm. One of the most common terminations used when driving a long coaxial cable with an LSTTL gate is shown in Fig. 1. This set-up is unsuitable for a HCT bus driver, since the termination provides a poor impedance match, and requires a current sinking capability of 20 mA.

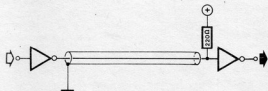
An improved termination circuit is shown in Fig. 2: this ensures reliable signal transmission for cables up to 15 m. Note that the 1k $\Omega$  pull-up resistor is only required when

the driver is an open collector gate or buffer.

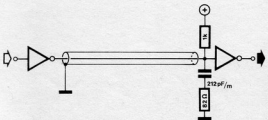
Flat ribbon cable often introduces considerable crosstalk between wires, especially when terminated in HC(T) gates, which form a high input impedance. In general, a flat ribbon cable should not be longer than about 60 cm, but longer runs are possible when individual wires are separated by grounded wires (1.8 m max.), or when each wire is terminated with a 1 k $\Omega$  pull-up resistor (1.2 m). A combination of these methods makes it possible to use flat ribbon cables with a length up to 2 m, but this is also attainable without ground wires—see Fig. 3. The combined use of this termination network and grounded wires in the flat ribbon cable should enable a cable length of about 5 m.

St

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3



87455

After a longish absence from the semiconductor scene, the *tunnel diode*, also called *Esaki diode*, after its Japanese inventor, has been re-introduced thanks to the fact that it can be used to save energy. In the nineteen fifties and sixties, tunnel diodes found many applications mainly in RF circuits, where their rather special properties were exploited for making fast level detectors, oscillators, mixers, and the like. As compared with a normal diode, a tunnel type utilizes a semiconductor material with an extremely high doping level, causing the depletion layer between the p-n junction to be roughly a thousand times narrower than that in even the fastest of normal silicon diodes. When the tunnel diode is forward biased, *tunnelling* of the electron stream occurs across the p-n junction. Tunnelling in doped semiconductors is a phenomenon not readily explainable on the basis of traditional atomic theory, and can not possibly be expounded in this brief article.

When measuring the correlation between a tunnel diode's forward voltage,  $U_f$ , and current,  $I_f$ , it will be found that the device possesses a *negative resistance* characteristic between the peak voltage,  $U_p$ , and the valley voltage,  $U_v$ , as shown in Fig. 1. Thus, if the diode is operated in the shaded section of its  $I_f$ - $U_f$  curve, the

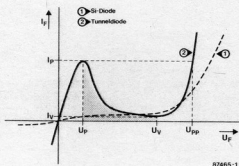
forward current falls as the voltage rises. The resistance of the diode is undisputedly negative, and usually given as  $-R_d$ .

The present design exploits the above property of tunnel diodes by having a series connected set of these devices charge a battery with the aid of solar energy. As seen in Fig. 2, seven or more Gallium-Indium Antimonide (GISp) tunnel diodes are series connected and fitted on a large heatsink, which does not serve to dissipate their power (tunnel diodes get colder as  $U_f$  rises), but to effectively accumulate solar, or otherwise applied, heat, whose energy is converted into a charge current for the NiCd battery.

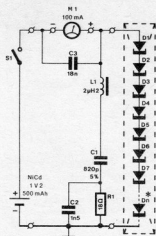
The operating principle of this unique design is remarkably simple. If a normal, pure, resistance,  $R$ , *discharges* a battery with current  $I = V/R$ , a negative resistance *charges* the same battery, since the sign of  $I$  reverses:  $-I = V/-R$ . Similarly, when a normal resistance *dissipates*  $P = I^2 R$  watts, a negative resistance *delivers* this wattage into the load:  $P = -I^2 - R$ . When the load is itself a voltage source with fairly low internal resistance, the negative resistance must, of course, output a higher voltage for the charge current,  $I_c$ , to flow:

$$I_c = \delta \left[ \sum (U_f) - U_{bat} \right] / \sum (R_d) + R_{bat}$$

1



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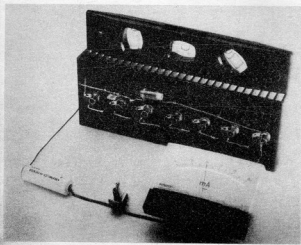


\* see text

D1...D7 = BA 7891 NG

From the notation  $\sum(R_d)$  it is immediately seen that all diodes in the series chain must be operated in the  $-R_d$  area, because any single diode with a  $+R_d$  characteristic would cancel the object effect. To ensure that all diodes exhibit a negative resistance, a simple test circuit can be made as shown in Fig. 3. Note that the meter must be capable of indicating the direction of the current, since it may well happen that a particular diode has such a high  $I_p$ - $I_v$  ratio (*tunnel slope*) that the battery is unintentionally charged on applying a small forward bias. The test must be carried out at

an ambient temperature below  $7^\circ\text{C}$  (use a cleared out refrigerator), and the  $U_f$ - $I_f$  curve is noted for every individual diode by carefully raising the forward bias with the aid of the potentiometer, and recording the resultant values of  $I_f$ , read from the meter. Put an FM radio nearby to make sure that the diode under test does not oscillate at 94.67284 MHz ( $F_{res}$  for GISp at doping level  $10^{-7}$ ). If it does, it is unsuitable for the present application. Establish the range of  $U_f$  that ensures  $-R_d$  for *all* diodes. Depending on the production tolerance of the diodes in the available lot, this span may be as restricted

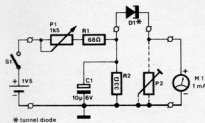




as, say, 180 to 230 mV. Calculate the number of diodes required for charging the battery with its nominal current: for the above range of  $U_f$ , at least 7 diodes must be series connected to give a charge current of about 45 mA if they are heated to  $[-\sum(R_n)I][\partial(R_n)/\partial T] - R\theta$ .  $1/(T_0 + T_s)^2$ , or about  $35^\circ\text{C}$  if the thermal resistance of the heat sink is less than  $3.5\text{ K/W}$ , and if it is positioned in bright sunshine ( $T_s \approx 26^\circ\text{C}$ ). To obtain the highest possible efficiency from this NiCd charger, the heatsink must be black for optimum heat transfer to the diodes, and it should not

be magnetic, since any external field, induced or magnetic, causes disuniform agitation of the charge carriers in the tunnels, and hence gives rise to the so-called *duct* effect; electrons tend to be dislodged from the p-n junction on the substrate, and consequently accumulate on the diode terminals, causing possibly dangerous potentials with respect to the metal enclosure. Many tunnel diodes Type BA7891NG are, unfortunately, quite sensitive to external fields, and practice has shown that they must be kept horizontal with respect to the earth's surface to preclude

3



87465-3

ducting when forward bias is applied. from an idea by J Freshwater & C Sanjay.

## 44

## SMD HEADPHONE AMPLIFIER

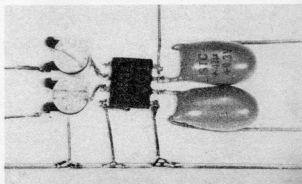
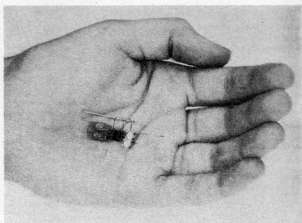
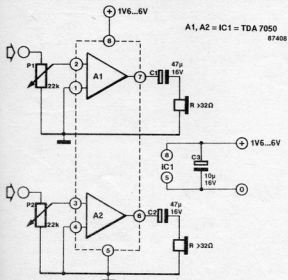
Although the use of SMDs (surface mount devices) is not yet widespread among electronics hobbyists, and the availability of these parts is still problematic in certain areas, there appears to be no way of stopping the ever increasing miniaturization of chips and circuits. A good instance of this happening at an accelerating pace is the Type TDA7050 headphone amplifier, which used to be available in a standard DIL enclosure, but is currently only manufactured in SMA technology.

The Type TDA7050 is a complete stereo amplifier with a gain of 26 dB and an output power of  $2 \times 75\text{ mW}$ . As seen in the circuit diagram, two electrolytic capacitors are required to block the offset voltage at the amplifier outputs. It is also possible to set up the amplifier in a bridge configuration to obtain an output power of 150 mW: simply omit the capacitors, and connect pins 2 and 4 to ground. Pins 1 and 3 are connected to form the amplifier's input, while the loudspeaker is connected

between pins 6 and 7. The current consumption of the chip at maximum output power is of the order of 100 to 150 mA, while the quiescent current amounts to a mere 5 mA. The amplifiers should be terminated

in  $32\Omega$ , a common value for modern headphones. The supply voltage is normally 4.5 V, and pins 6 and 7 are at half the supply potential during quiescent operation.

St



by W Teder

The basic dynamic characteristic of a chord can be analysed as a fast rising, needle-shaped pulse with a virtually exponential decay—see Fig. 1. This typical amplitude characteristic can only be faithfully reproduced by an amplifier if this is operated well below its overload margin, and that, many guitar players know, generally results in too low an average sound level. Also, when it is desired to use a high volume setting, the distortion soon rises to an unacceptable level. Although the above difficulty is widely remedied by means of a tightly set compressor or limiter, the sound may then lack the required aggressiveness. This circuit is expected to give better results than most other limiters, because it is only active in the upper range of the dynamic characteristic.

The gain of the preamplifier set up around IC<sub>1</sub> is adjustable with P<sub>1</sub>. The inverting input of the opamp is grounded via the drain-source junction of n-channel FET T<sub>1</sub>, which operates as a voltage-controlled resistance here, and is driven with a negative gate voltage derived from the limiter's output signal. The gain of the opamp is therefore inversely proportional to the gate voltage of the FET, whose drain-source resistance is reduced as the gate voltage becomes more negative. Network R<sub>5</sub>-C<sub>4</sub> effectively reduces the distortion incurred by the regulating action of the FET. It may be necessary to redimension R<sub>5</sub> and C<sub>4</sub> to compensate for the tolerance on the FET—use an oscilloscope and a function generator to find the optimum values for these components while the circuit is being arranged to operate at maximum compression.

The limiter is fairly simple to align. Apply a 1 kHz, 150 mV input signal to the input, and monitor the output signal with an oscilloscope. Adjust P<sub>1</sub> such that maximum amplification is obtained with virtually no distortion. Increase the input amplitude to 300 mV: this is

likely to make some distortion noticeable. Carefully turn P<sub>1</sub> back until the distortion is reduced to an acceptable level. In some instances, when the distortion remains too high whatever the setting of P<sub>1</sub>, it may be necessary to replace T<sub>1</sub>, since the Type BF256C is

manufactured with a relatively loose tolerance.

The proposed limiter leaves the lower dynamic range unaffected, while slightly compressing the peak amplitudes in the input signal. Optimally aligned, it suffers none of the notorious side-effects such as "noise

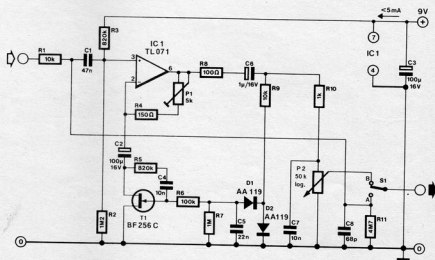
breathing" and clipping commonly associated with other units, while it enables guitar amplifiers to be driven 3 dB harder without producing appreciable distortion.

D

1



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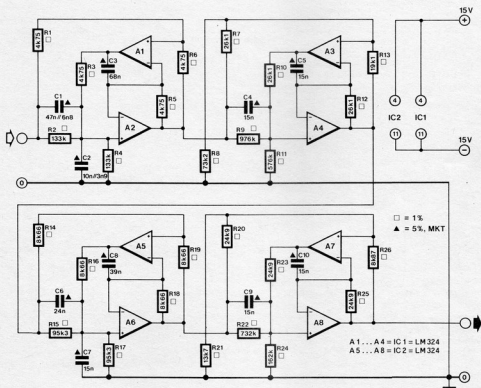


Morse, or CW (continuous wave), is still widely used thanks to the fact that the necessary equipment can be kept relatively simple, and therefore inexpensive, if the operator is sufficiently trained in selective listening. A morse decoding computer, however, requires an adequately filtered

input signal, because it lacks the noise discriminating capability of the human ear. Some receivers can be upgraded with a 250 Hz IF filter for this purpose, but such an extension is usually well beyond the financial reach of most radio amateurs. The filters discussed here operate in the audible fre-

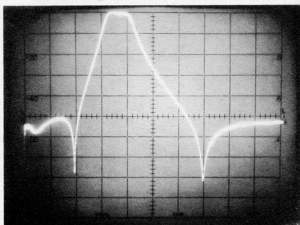
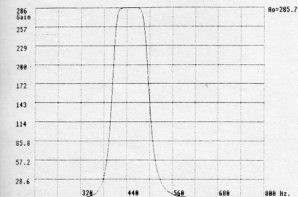
quency range, and compare favourably with far more expensive types for 455 kHz. Figures 1 and 2 show the circuit diagram and the typical response of an eighth-order inverse Chebishev filter which has been optimized for non-computer using listeners. The filter of Fig. 3 is less complex,

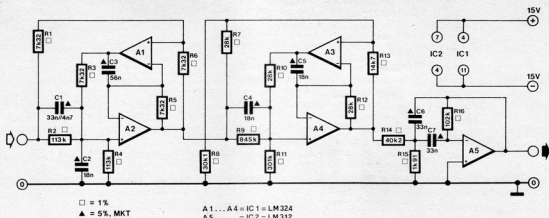
and intended for driving a computer. The associated frequency response is shown in Fig. 4. Both filters were designed with *Eldesign IIe*, an advanced filter design program for the BBC micro. The inverse Chebishev response gives a smooth pass-band, while the characteristic ripple ends up in



87489-1

2





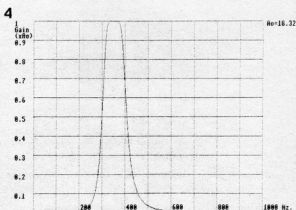
87489-3

the stop band. This ensures the required phase stability in the pass-band, which is a must for processing burst-like signals such as morse.

Prototypes of the filters gave excellent results: normally hardly audible signals could be recovered for reliable decoding. The supply for the filters is preferably a symmetrical 15 V type to ensure an optimum dynamic range. Do not use any other opamp than the LM324, since types with a higher cut-off frequency may give rise to oscillation. Note that  $C_1$  in Figs. 1 and 3, and  $C_2$  in Fig. 1, is a

parallel combination of two capacitors from the E12 range of values, while all resistors used are from the E96 range. Should any of the filter sections persist in its tendency to oscillate, either one of the even-numbered opamps may have to be dimensioned for a slightly different roll-off point by connecting a 100 pF capacitor across the output and the - input, and a 390  $\Omega$  resistor between the - input and junction  $C_3$ - $R_5$  (-A<sub>1</sub>) (example refers to opamp A<sub>2</sub>).

B



## 47

## WIEN BRIDGE OSCILLATOR

This AF oscillator can be built with only one active component, and draws so little current that it is conveniently fed from a 9 V (PP3) battery.

The basic circuit of the Wien bridge oscillator is shown in Fig. 1. The oscillator consists of two sections, namely the opamp plus  $R_3$ - $R_4$  which determine the amplification factor, and positive feedback network  $C_1$ - $R_1$ - $C_2$ - $R_2$  which enables the circuit to oscillate. This network is composed of a low-pass section  $R_2$ // $C_2$ , and a high pass section  $R_1$ + $C_1$ . The phase difference incurred in these is nulled at the frequency of oscillation, when the filters form a pure ohmic potential divider

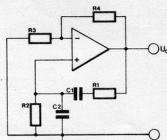
with an attenuation of 3. Therefore, the opamp must have an amplification of 3, to keep the overall amplification at unity, so that the oscillation is maintained. The output frequency,  $f_o$ , of the oscillator is

$$f_o = 1 / (2\pi \sqrt{R_1 R_2 C_1 C_2}) \quad [\text{Hz}]$$

but only if  $R_1 \approx R_2$  and  $C_1 \approx C_2$ . In the practical design shown in Fig. 2, the oscillation frequency is about 1,000 Hz.

Both the inverting and the inverting input of the opamp in Fig. 1 must be held at half the supply voltage to ensure minimum current consumption if the oscillator is to be fed from a battery. Figure 2 shows how this

1



87615-1

is realized in the practical version of the Wien bridge oscillator. Here, resistors  $R_2$  and  $R_3$  from Fig. 1 are seen as  $R_{2a}$ - $R_{2b}$  and  $R_{3a}$ - $R_{3b}$ , respectively, connected as voltage dividers. This

can be done with impunity, because the voltage source is a virtual short circuit for alternating voltages, and there is also  $C_3$  as an effective decoupling device. For an alternating

voltage, therefore, the resistors are parallel combinations. Evidently,  $R_{2a}$ ,  $R_{2b}$ ,  $R_{3a}$ , and  $R_{3b}$  have two times the calculated resistance of the respective components  $R_2$  and  $R_3$  in Fig. 1. The amplification of the opamp is adjustable with  $P_1$ , which should be set for reliable oscillation at virtually no distortion of the output sine wave. When the oscillator is properly aligned, the distortion should be less than 0.1%.

The use of the Type TLC271 CMOS operational amplifier results in a current consumption of only 0.32 mA at  $U_o = 6 V_{pp}$ . It is possible to use a special low-power opamp such as the type OP-22 biased with a resistance of 1 M $\Omega$  to reduce the current consumption to

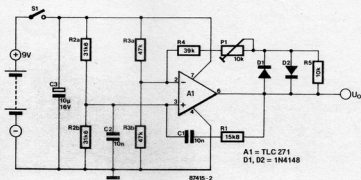
0.1 mA. However, this will cause the oscillation frequency to be limited to 1,000 Hz, due to the reduced slew rate at very low

bias settings, which in turn give rise to a strong increase in the distortion level.

Sv

PMI Application Note AB111.

2



A1 = TLC271  
D1, D2 = 1N4148

87415-2

48

## PRECISION CRYSTAL OSCILLATOR

from an idea by R Shankar

When designing crystal oscillators, it is good practice to ensure minimum capacitance of the active element(s), since any parasitic loading of the crystal is bound to derate the overall stability to some extent. This forms the underlying principle of the design described here, albeit that good results are also obtainable when an additional load capacitance is connected in parallel with the existing parasitic capacitance,

but only if the former is known to possess a low loss factor and a low temperature coefficient, i.e., if it is a very high quality capacitor (and possibly difficult to obtain).

The oscillator proposed here is a Pierce type, in which the crystal operates in parallel mode. The input is formed by a bootstrapped source follower, DG MOSFET  $T_1$ , which has a parasitic capacitance of only 1 pF. RF transistors  $T_2$ - $T_3$  are set up as a cascode amplifier. A type BF494 transistor is used in

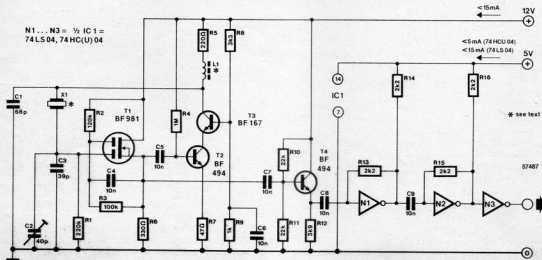
the  $T_2$  position because of its low B-E capacitance (0.15 pF typ.), which ensures a low output parasitic capacitance. The oscillator signal is taken from the source of  $T_1$ , buffered in  $T_4$ , and made logic compatible with the aid of gates N-N<sub>3</sub>. The optimum inductance of  $L_1$  is approximated with  $L_1 = 1/f$ , where the inductance and frequency are in milli-henries and megahertz respectively. Example: for  $f = 10$  MHz,  $L_1$  works out at 100  $\mu$ H. Trimmer  $C_2$  serves to accurately tune the crystal

oscillator to the required frequency. The oscillator works well up to about 20 MHz.

Finally, although the dissipation of the crystal is not expected to give rise to instability, it is still a good idea to keep an eye on its output amplitude so as to preclude the protective diodes in  $T_1$  being activated and causing unacceptable instability. If required,  $R_7$  is altered until the signal amplitude at the emitter of  $T_1$  is less than 1 V<sub>pp</sub>.

B

N1...N3 = 1/2 IC1 =  
74LS04, 74HC(U)04



by C Sanjay

In many cases it may be necessary to switch between two or more aerials with minimum loss in the RF signal. Though this is not generally a problem at low frequencies, it becomes a serious one when the relevant signal is in the VHF/UHF range (50-960 MHz). The electronic switch described here keeps the switching losses minimal by making use of PIN diodes. PIN diodes are essentially current controlled resistors with properties that make them suitable for switching and attenuating RF signals. They differ from most other types of diode in that rectification of the input signal only occurs below a certain limiting frequency. Above this frequency, the resistance of a typical PIN diode will change from  $1\Omega$  to  $10,000\Omega$  when the control cur-

rent is reduced from 100 mA to  $1\mu\text{A}$ .

The circuit can switch up to four aerials, and is composed of two functional parts: the RF switching section, mounted onto the aerial mast, and the power supply & control section, kept near the receiver. In this way, the cost of setting up a multi-aerial system is reduced to some extent thanks to the use of a single download cable, instead of as many as there are aerials.

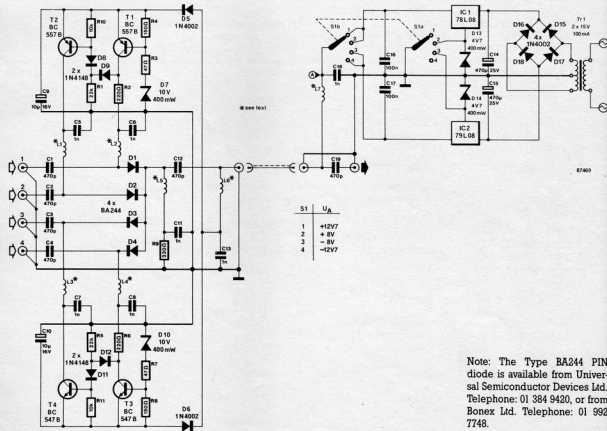
The required aerial is selected by biasing the corresponding PIN diode into conduction. Which of the four diodes conducts depends on the level and the polarity of the voltage applied to the switching unit via the download cable to the receiver. When, for example, input 1 is selected with  $S_1$ , the voltage on the core of the download cable is +12.7 V with respect to the cable screen,

and can not reach the circuit around  $T_1$  and  $T_4$  because  $D_4$  does not conduct. The level of the positive voltage causes zener diode  $D_7$  to conduct, and so provides a bias for  $T_1$ , driving it into saturation.  $T_1$  in turn provides the requisite bias for PIN diode  $D_1$ , and at the same time prevents  $T_2$  from conducting. Input 1 is thus connected to the common output of the switching unit, through  $D_1$ . If  $S_1$  is set to position 2, the supply voltage on the download cable falls to 8 V, which is insufficient for  $D_7$  to conduct.  $T_1$  now remains switched off, and  $T_2$  is driven into saturation, providing the required bias current for the associated PIN diode,  $D_2$ . Diodes  $D_8$  and  $D_9$  prevent  $D_1$  from being biased through  $R_1$  and the base-emitter junction of  $T_2$ . Input 2 is thus connected to the common output through  $D_2$ . Similarly, when the voltage on the core of the download cable

is negative with respect to the screen, the circuit around  $T_3$  and  $T_4$  works as outlined above, with either  $D_3$  or  $D_4$  conducting, depending on the level of the voltage ( $-8$  or  $-12.7$  V).

Inductors  $L_1$ - $L_4$  prevent the RF signal from being earthed anywhere in the circuit, while  $L_7$  prevents it from being short-circuited in the power supply. For VHF applications of the circuit,  $5\mu\text{H}$  inductors or chokes should be used in the  $L_1$ - $L_4$  positions, while  $2\mu\text{H}$  types are required for UHF operation. The RF signal from the selected aerial is passed to the receiver input through  $C_{19}$ , which serves to block the direct voltage. In case balanced aerials are to be switched, their outputs must first be made unbalanced and, if necessary, transformed to  $75\Omega$ , using a balun.

Th

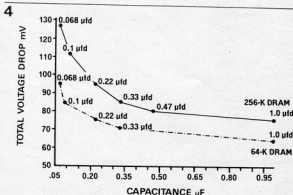
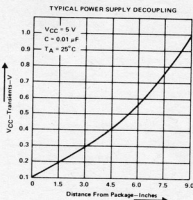
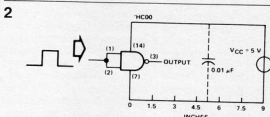
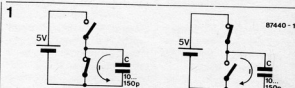




Failing to heed the importance of adequately decoupled supply rails is one of the most serious mistakes a constructor of digital circuits can make. Two important facts necessitate a reappraisal of the effectiveness of decoupling: the introduction of the fast HC and HCT series of CMOS chips, and the general availability of ever larger dynamic RAM (DRAM) devices. The 41256 256Kbit DRAM and 6264 CMOS SRAM, for instance, have become commonly used integrated circuits, available at relatively low cost. The fast spreading use of the new CMOS series of logic circuits has created the widely heard misunderstanding that these devices can be used without paying the least attention to decoupling of the supply lines. However, a reduced current consumption relative to TTL devices is by no means a carte blanche for designers to skimp on decoupling provisions, as will be seen below. Why does a logic circuit draw current? The current consumption of TTL chips goes mainly on account of indispensable, internal, resistors. CMOS structures are complementary, and theoretically consume no current at all in the *static* mode. As soon as any kind of switching is to be done, both by TTL and CMOS circuits, the charge of the capacitance at the output must be reversed as illustrated in Fig. 1. The switch currents internal to the IC are only a fraction of those required for the load capacitance, and can, therefore, be disregarded, except in the case of counters. TTL and CMOS circuits thus consume an equal peak current during switch operations. Decoupling capacitors are fitted direct to the IC supply terminals to prevent the instantaneous supply voltage from briefly dropping to an unacceptable level when the switching takes place. The graph in Fig. 2 is reproduced from a Texas Instruments data-book, and shows the correlation between the capacitor-to-package distance and the peak amplitude of the spikes on the

supply line to a typical HCMOS gate. This shows beyond doubt that decoupling capacitors must be fitted as close as possible to the IC supply terminals, to rule out the stray inductance of supply tracks on the PCB, however neatly these may run in parallel. Often, tuned circuits are designed with long supply tracks and a wrongly placed decoupling capacitor. Any spike is then subject to ringing effects, which further deteriorate the operation of the logic circuit in question. Not surprisingly, Mullard recommend a multi-path supply track when it is impossible to fit the decoupling capacitor close to the IC. This solution is called a *grid structure*, and is definitely preferable to creating relatively wide, single tracks—see Fig. 3. The value of the decoupling capacitor must be based on the foreseeable number of IC outputs that are *simultaneously* active. A conventional starting point is 20 to 100 nanofarad for every three ICs. Further reflection on this theme leads to the conclusion that the supply for a 256Kbit DRAM is far more difficult to decouple than that for, say, a 16 Kbit DRAM. Fortunately, the problems are not as serious as one would expect. In practice, the size of the chip carrier, and hence the parasitic capacitance, is constantly reduced by the manufacturers, whose foremost aim is to ensure optimum response of the device at high operating frequencies. Certain DRAM manufacturers recommend the use of 330nF decoupling capacitors (see Fig. 4), but in practice no problems evolved from the use of the standard value of 100nF.

W





From an idea by R de Haan

This circuit activates a relay upon detecting the absence of light on an LDR (light dependent resistor). It is particularly well suited to control outside lighting as used for driveways and garage entrances.

Contrary to its normal use as an astable or monostable multivibrator, the Type 555 IC in this circuit functions as a comparator. To explain this rather unusual application, it is necessary to note that the operation of a 555 is normally as follows: the output goes high upon receipt of a trigger (start)

pulse on input pin 2. This pulse is a voltage whose level is lower than  $\frac{1}{2}$  of the supply voltage. The output goes low again when the voltage at the second input, pin 6, has briefly exceeded  $\frac{1}{2}$  of the supply level. In the present design, the second input is not used, but the output of the chip can none the less revert to the low state, since pin 6 is connected direct to the positive supply rail. This set-up is accounted for by the accompanying Table, taken from the 555's data sheets. In principle, the supply voltage for the circuit must equal the coil voltage of the relay. Do not

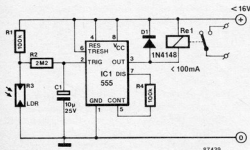
apply more than 16 V, however, as this may damage the 555. The current consumption of the circuit is 4 mA, exclusive of the relay, at a supply level of 12 V. Components  $R_2$  and  $C_1$  ensure a delay of about 10 s before the relay is energized, so that the circuit is rendered insensitive to rapid changes in the light intensity.

Basically, the circuit has no hysteresis effect. However, when the supply is not regulated, the actuation of the relay will lower the supply level somewhat. This lowers the internal threshold of the IC, since the trigger point is de-

fined as  $\frac{1}{2}$  of the supply level (pin 2). Therefore, the hysteresis of the circuit can be dimensioned as required by fitting a resistor in series with the supply. It is also possible to fit a resistor between pins 5 and 7 of the 555, as shown in the circuit diagram. The amount of hysteresis is inversely proportional to the value of the resistor, and 100K is a reasonable starting point for experiments.

The sensitivity of the trigger circuit can be controlled if  $R_1$  is replaced with a 1M0 potentiometer or preset.

W



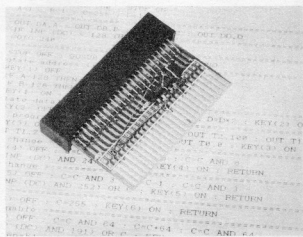
NE555

FUNCTION TABLE

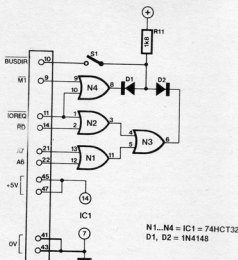
RESET (4)	TRIGGER VOLTAGE (2)	THRESHOLD VOLTAGE (6)	OUTPUT (3)	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	$< \frac{1}{2} V_{DD}$	Irrelevant	High	Off
High	$> \frac{1}{2} V_{DD}$	$> \frac{1}{2} V_{DD}$	Low	On
High	$> \frac{1}{2} V_{DD}$	$< \frac{1}{2} V_{DD}$	As previously established	

The majority of MSX computers do not require a BUSDIR (bus direction) signal from add-on circuits plugged into slots. A problem arises, however, if the extension circuits published in *Elektor Electronics* are used in conjunction with, for example, a Sanyo MSX machine, which has a few peculiarities in its external I/O concept. In general, the more slots on a MSX computer, the higher the probability that either one of, or both, these circuits are required to be able to use the home-made extensions. Two solutions are offered to provide for the BUSDIR signal.

One is usable for the *Universal I/O Bus* and the *I/O & Timer Cartridge*, the other for the *Cartridge Busboard*. Each of these circuits consists of one IC only. Circuit A is used with the two I/O extensions, and is readily incorporated in the computer, at a suitable location near the slot that receives the extension. If necessary, all slots on the computer are fitted with this circuit, but this makes it impossible to utilize cartridges that do supply a BUSDIR pulse, unless  $S_1$  is included to disconnect the output of  $N_1$  from slot pin 10. Note, however, that this switch must not be operated when the



A



N1...N4 = IC1 = 74HCT32  
D1, D2 = 1N4148

computer is on.

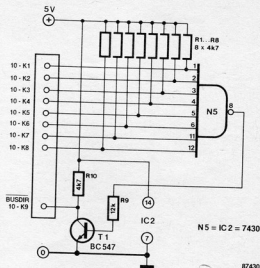
As I/O range 40k-FFh is reserved for the computer-resident hardware, address lines A<sub>6</sub> and A<sub>7</sub> must be low for the selection of external I/O circuitry. Moreover, IOREQ and RD must be low to ensure that BUSDIR is only active when the CPU reads data from an I/O device. Interrupts from an external device can only be processed correctly when BUSDIR is low in response to M1 and IOREQ being low also. This requires an OR function for logic low levels:

BUSDIR =

M1 · IOREQ + IOREQ · RD · A<sub>7</sub> · A<sub>6</sub>  
If you are hesitant about opening the computer to install circuit A, you may consider the use of a part of the EPROM cartridge board to hold the 74HCT32 as shown in the accompanying photograph. Note that the 50-way track connector plugs straight into a computer slot, and that a slot connector is fitted at the other side of the "adaptor-PCB" to receive cartridges.

Circuit B is intended for use on the Cartridge Busboard. Its

B



N5 = IC2 = 7430

87430

function is to pass BUSDIR pulses from cartridges to the computer. To this end, it is necessary to first break the interconnecting tracks between slot pins 10 so as to make all cartridge BUSDIR outputs separately available for wiring to 8-input NAND gate N<sub>5</sub>. Inverter T<sub>1</sub> turns this simple add-on unit into an 8-input OR gate for logic low levels. The collector of this transistor is wired to pin 10 of K<sub>8</sub> on the busboard.

It may well happen that both circuit A and B are required for a specific I/O arrangement. In

that case, it is suggested to fit circuit A on one slot of the Cartridge Busboard, and consequently use only that slot for external I/O. Pin 8 of N<sub>4</sub> is then connected direct to the relevant input of N<sub>5</sub>.

R

Note: articles in the series *MSX Extensions* were published in the following issues of *Elektor Electronics*:

January 1986, February 1986, March 1986, January 1987, March 1987, April 1987.

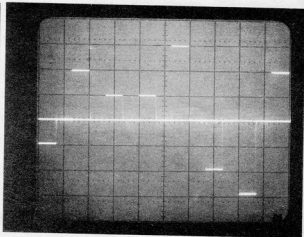
## 54

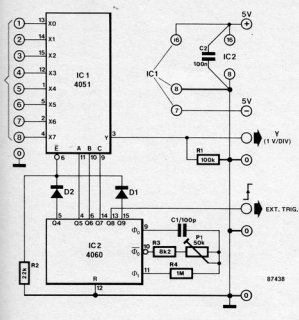
## 8-CHANNEL VOLTAGE DISPLAY

Simultaneously monitoring the trends of 8 slowly varying voltages is normally very difficult, if not impossible, even with the aid of 8 analogue or digital voltmeters. This circuit turns a common oscilloscope into a versatile 8-channel display for direct voltages. The trend of each of the 8 input levels is readily observed, albeit that the attainable resolution is not very high.

The circuit diagram shows the use of an 8-channel analogue multiplexer, IC<sub>1</sub>, which is the electronic version of an 8-way rotary switch with contacts X<sub>8</sub> and pole Y. The relevant

channel is selected by applying an binary code to the A-B-C inputs. Example: binary code 011 (A-B-C) enables channel 7 (X<sub>8</sub> → Y). The A-B-C inputs of IC<sub>1</sub> are driven from three successive outputs of binary counter IC<sub>2</sub>, which is set to oscillate at about 50 kHz with the aid of P. As the counter is not reset, the binary state of outputs Q<sub>6</sub>, Q<sub>5</sub> and Q<sub>7</sub> steps from 0 to 7 in a cyclic manner. Each of the direct voltages at input terminals 1 to 8 is therefore briefly connected to the Y input of the oscilloscope. All eight input levels can be seen simultaneously by setting the time-





base of the scope in accordance with the time it takes the counter to output states 0 through 7 on the  $Q_3$ ,  $Q_4$ ,  $Q_7$  outputs. The correct starting time for the oscilloscope trace is ensured by using the  $Q_8$  output of the counter to supply the trigger pulse. Diodes  $D_1$  and  $D_2$  provide for some space between adjacent bars on the display, and create a horizontal reference line.

The timebase of the scope should be set to 0.5 ms/div, and triggering should occur on the positive edge of the external signal. Set the vertical sensitivity to 1 V/div. The input range of this circuit is from -4 V to +4 V, and connected channels are terminated in about 100K. Adjusting the 8-channel voltage display is straightforward. Simply select the previously mentioned scope settings, and adjust  $P_1$  to make all 8 channels

visible over the full width of the scope screen—see the accompanying photograph.

The circuit has a modest current demand of less than 5 mA from a simple  $\pm 5$  V supply, or from two 4.5 V flatpack batteries.

Th

# 55

## TRACKING WINDOW COMPARATOR

by H Gulitz

The use of comparator circuits in many different appearances and practical realizations is common in a wide variety of electronic control and measurement systems. Usually, the voltage from a sensor device is fed to a comparator which, as its name implies, compares the

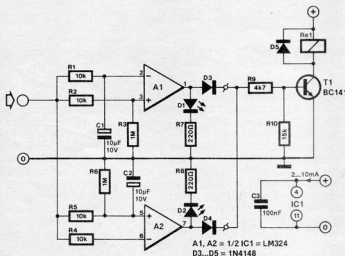
measured level,  $U_{in}$ , with a fixed reference,  $U_{ref}$ , and produces a negative output (0) or positive output (1) when  $U_{in} < U_{ref}$  and  $U_{in} > U_{ref}$ , respectively. A *window comparator* can be made by connecting two comparators with different reference levels, which define the upper and lower limit of the switching range.

In practice, these references are usually adjusted with presets to dimension the window as required. This arrangement makes it impossible, however, to automatically shift the window up or down in accordance with, say, ambient light conditions to be measured with a light dependent resistor. This circuit has no fixed

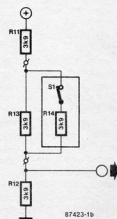
threshold levels, but derives its reference from the measured signal, so that slow changes in this cause the window to track along.

Capacitors  $C_1$  at the inverting input of  $A_1$ , and  $C_2$  at the non-inverting input of  $A_2$  store the input voltage. When the voltage at the non-inverting input of  $A_1$  rises, this opamp toggles. The

1a



b



associated inverting input lags, this change because of the delay introduced by the capacitor. LED D<sub>1</sub> lights. The process is similar in the A<sub>2</sub> section of the circuit when the input voltage drops. This is indicated by LED D<sub>2</sub> lighting.

Diodes D<sub>2</sub> and D<sub>4</sub> form an OR function to actuate a simple relay driver set up with T<sub>1</sub>. The relay is energized when the circuit detects a fast change in the input voltage. The ability of the

circuit to accept a variable input voltage makes it suitable for use in burglar alarms—see Fig. 1b. Several break contact arrangements  $R_{13}$ - $S_1$ - $R_{14}$  may be connected in series and to the input of the window comparator. Alarm relay  $Re_1$  is activated when either  $S_1$  is opened or  $S_1$ - $R_{14}$  is bypassed. To prevent burglars from fooling the alarm,  $R_{14}$  must be fitted into  $S_1$ , because no alarm signal is given when only  $S_1$  is shorted.

The sensitivity of the tracking window comparator is defined by the ratios  $R_2/R_1$  and  $R_3/R_4$ . The relevant component values indicated in the circuit diagram give 1:100 ratio, so that, for example, a fast change of 30 mV is detected when the input voltage is 3 V. The sensitivity also depends on the input voltage. Although the circuit can in principle handle any input between 0 V and the supply level, the ICs used

give reliable operation only when driven between 1 and  $U_b - 1$  volt.

The tracking window comparator is preferably fed with a supply between 5 and 15 V. Its current consumption, inclusive of the LEDs but exclusive of the relay, is 10 mA maximum (note that the relay can be fed separately).

## 56

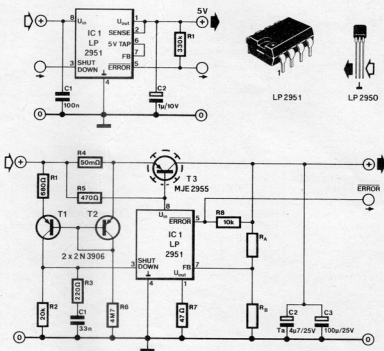
## LOW VOLTAGE DROP REGULATORS

The fast spreading incorporation of CMOS, HC and HCT chips has created a need for voltage regulators with a very low internal drop to enable powering CMOS-based equipment from a set of batteries delivering 6 V. The recently introduced Types LP2951 and LP2950 from National Semiconductor are micropower voltage regulators with a variable output voltage of 1.24-29 V and a fixed output voltage of 5 V, respectively. The former features an internal voltage divider with a 5 V tap bonded out to a pin, a logic compatible shutdown input, and an open-collector ERROR output which warns of a low output voltage, often due to an insufficient battery voltage at the input. The ERROR output is extremely useful for an early warning system that arranges for a microprocessor to be reset properly before the supply voltage falls to a level that would upset the operation of the system it controls.

The voltage drop across the LP2951 is only 0.4 V at a load current of 100 mA, so a 6 V battery pack can be used to power a 5 V circuit. The quiescent current drain of the regulator is about 12 mA at an output current of 100 mA. This is fairly high as compared with a conventional regulator from the 78XX family, and mainly due to the internal series regulator transistor being driven into saturation, which causes it to have a relatively low current amplification factor (the base

current flows into the ground return line, instead of into the output load, as with the typical 78XX regulator).

The application circuit shown in Fig. 1a should be fed from an input voltage of more than 5.4V while its maximum output current is 100 mA. Note that both the LP2950 and LP2951 feature internal current and thermal limiting circuits. The decoupling capacitor at the output of the regulator should be a good quality tantalum type, fitted as close as possible to pins 1 and



87428.1

4. At relatively low output currents, less capacitance is required in this location. For currents below 10 mA, 0.33  $\mu\text{F}$  is satisfactory, while the minimum value is 0.1  $\mu\text{F}$  for currents below 1 mA. These values apply to an output voltage of 5 V; for lower voltages, more output capacitance is needed.

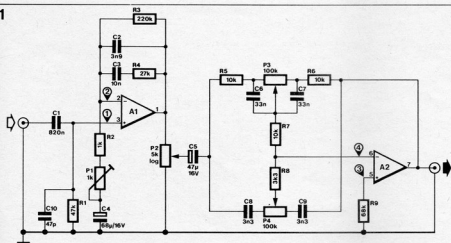
The circuit in Fig. 1b is a 2 A low dropout regulator based on the LP2951. The output voltage is calculated from

$$V_o = (1 + R_A/R_B)1.23V$$

where L23 stands for the voltage at the feedback input, pin 7. For an output of 5 V,  $R_A$  and  $R_B$  may be omitted, and the feedback input pin 7 can be connected direct to the 5 V tap (pin 6) output. The sense input, pin 2, is then connected to the  $V_o$  rail. In this application,  $V_{in}$  must be at least 0.5 V higher than  $V_o$ .

*National Semiconductor applications*

1



A1, A2 = IC 1 = TLC272



This design answers the need for an inexpensive, yet good quality, preamplifier equipped with a tone control section.

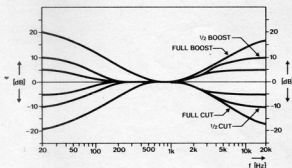
Fig. 1 shows the circuit diagram. The amplification of the input stage set up around opamp A<sub>1</sub> is adjustable between 10 and 20 with preset P<sub>1</sub>. The 0 dB level at the input is 50 mV, while the input impedance and capacitance are 47 K $\Omega$  and 47 pF, respectively to enable ready connection of most record players and cassette decks. The tone control section is a standard Baxan-

dall type with P<sub>3</sub> and P<sub>4</sub> as the respective bass and treble controls. The gain vs frequency curves for various settings of the tone controls appear in Fig. 2. Here the 0 dB level corresponds to 1 V.

The current consumption of this preamplifier is modest at about 5 mA. When the circuit is correctly balanced, the indicated measuring points should all be very nearly at ground potential. The circuit shown here must, of course, be duplicated to obtain a stereo preamplifier.

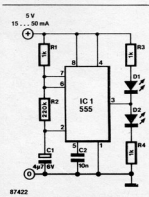
S

2



This application of the well-known Type 555 timer is intended for model railway enthusiasts wishing to construct a two-lamp flashing beacon with a minimum of components.

With reference to the circuit diagram, the number of LEDs need not be restricted to two: several may be connected in parallel to achieve a higher light intensity, but a total current consumption of 200 mA should not be exceeded to prevent the destruction of the output stages in the 555. Each LED added



should have its own current limiting resistor, similar to D<sub>1</sub>-R<sub>3</sub> or D<sub>2</sub>-R<sub>4</sub>.

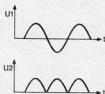
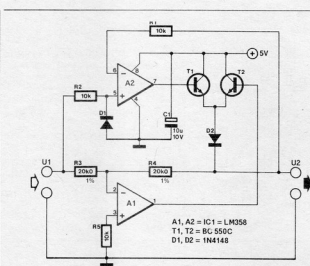
The flashing rate is defined with C<sub>1</sub>. The stated value of this component is likely to be optimum for applications in model railways. The supply voltage for the circuit is not critical, but should remain within the range from 5 to 10 V. With two LEDs fitted and a 5 V supply, the flashing circuit should consume less than 50 mA. The intensity of the LEDs can be adapted to individual pre-

ference by changing R<sub>3</sub> and R<sub>4</sub>, but too low resistance values should be avoided to prevent the destruction of the LEDs.

S

This precision rectifier operates from an asymmetrical supply, handles input signals up to  $3 V_{pp}$  and has a frequency range that extends from DC to about 2 kHz. Its amplification is unity, and depends mainly on the ratio  $R_4/R_1$ . Opamp  $A_1$  is connected as a voltage amplifier ( $A_v=1$ ),  $A_2$  as an inverting amplifier ( $A_v=-1$ ). Opamp  $A_2$ , transistor  $T_1$  and diode  $D_1$  ensure that the output voltage,  $U_2$ , is identical to the positive excursions of the input voltage,  $U_1$ . When  $U_1$  is positive, the output of  $A_1$  is held low at about 0.25 V, so that  $T_2$  is disabled and can not affect the rectified output signal.

Components  $R_2$  and  $D_1$  protect the pnp input stage in  $A_2$  against negative voltages, which are effectively limited to  $-0.6 V$ . For negative excursions of the input signal, the function of  $A_1$ ,  $T_2$  and  $D_2$  is similar to the previously mentioned compo-



S7416-1

nents. The peak output voltage of the rectifier circuit is determined mainly by the maximum output swing of the opamps

and the voltage drop across the transistors plus  $D_2$ : this amounts to about 3 V in all.

When the circuit is not driven, it

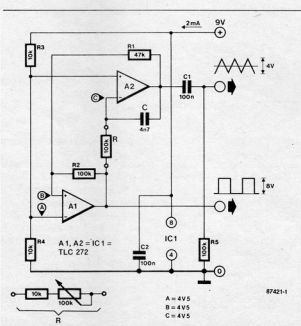
consumes about 1 mA, and is therefore eminently suitable for building into portable, battery-operated equipment.

Sv

This is a downright simple design for an AF function generator that supplies a rectangular and triangular signal, and can be fed from a single 9 V supply. The signal generator proper is a Type TLC272 dual CMOS opamp from Texas Instruments. This chip is remarkable for its low current consumption and wide operating range.

The circuit is essentially composed of two functional parts. Opamp  $A_1$  is connected to function as a Schmitt-trigger whose toggle point is set to 4.5 V, while  $A_2$  is an integrator that converts the rectangular signal from  $A_1$  into a triangular waveform.

The oscillation frequency of the circuit is fixed solely by the ratio  $R/C$  and can be calculated from  $f_0 = R_2/4RR_1C$ . Resistor  $R$  may be replaced by the combination of the 10K resistor and 100K potentiometer as shown to

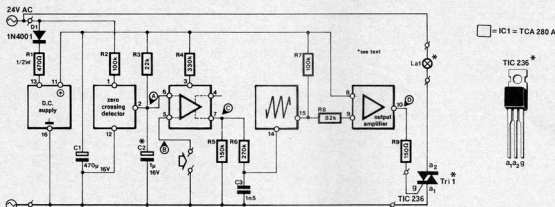


S7421-1

effect continuous adjustment of the output frequency within the AF signal band. The generator should not be terminated in less than 10K.

Sv

1

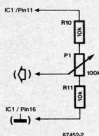


The circuit proposed here is suitable for fitting into slide projectors without a dimmer facility (24 V AC fed halogen lamps). With a few small alterations, it can also be used for dimming 12 V halogen lamps, but not those in a car, because these are fed from a DC source. The circuit shown in Fig. 1 is intended for operation from a 24 V AC supply, and can handle a lamp load of up to 150 W. For loads up to 250 W, the TIC236 should be replaced by a TIC246.

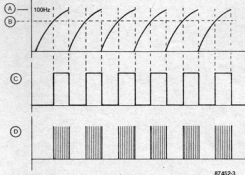
The illumination of the halogen lamp is controlled by applying a direct voltage to pin 5 of dimmer chip IC1. A voltage of +2.5 V gives maximum illumination, while +5 V results in the lamp being turned off completely. The lamp intensity control range—2.5 V to 5 V—can be extended upwards by decreasing the value of C2.

The TIC246 should be used when the circuit is to control a 12 V lamp that consumes more than 50 W. Figure 2 shows details of the connection of a potentiometer to the intensity control input of the TCA280A. Voltage divider R10-P1-R11 is fitted externally and can be fed from the stabilized voltage available at pin 11 of IC1. The minimum and maximum intensity of the lamp are determined by R10 and R11, respectively, so that the control range can be dimensioned to individual preference. When potentiometer

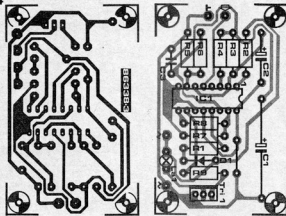
2



3



4



control is used, C2 must always be 100n.

Figure 3 shows the signal waveforms at various points in the circuit.

The halogen lamp dimmer is constructed on a printed circuit board as shown in Fig. 4. When

the lamp power is greater than 15 W, the triac should be fitted onto a heatsink, and the tracks to the a1 and a2 terminals should either be covered with solder, or strengthened with short lengths of wire.

#### Parts list

##### Resistors (± 5%):

- R1 = 470Ω; 16 V; axial
- R2/R7 = 100K
- R3 = 22K
- R4 = 330K
- R5 = 150K
- R6 = 270K
- R8 = 82K
- R9 = 150R

##### Capacitors:

- C1 = 470μ; 16 V; axial
- C2 = 1μ; 16 V; axial\*
- C3 = 1n5

##### Semiconductors:

- D1 = 1N4001
- Tri1 = TIC236 or TIC246\*
- IC1 = TCA280A

##### Miscellaneous:

- PCB Type 87452 (see Readers Services).
- Heatsink for Tri1.

\* See text

R

by S G Dimitriou

This versatile circuit serves to raise the average output power of an AF amplifier. Its simplicity makes it suitable for applications in intercom systems, public address and discotheque equipment, and also in various types of transmitter.

Compression of music and speech essentially entails reducing to some extent the dynamic range of the AF input spectrum in order to drive an AF power amplifier with a fairly steady signal level just below the overload margin, thus increasing the average output power of the system. However, some distortion is inevitably incurred in the process of amplifying the relatively quiet input sounds and attenuating the louder sounds. It is evident, therefore, that the control of the amplifier/attenuator function in the compressor determines to a large extent just how much distortion is introduced by the circuit.

Before inserting any type of

compressor in an AF signal path, due consideration should be given to the *attack time* i.e., the time it takes the circuit to detect and counteract a sudden increase in the amplitude of the incoming signal. Allowing for personal preference and the character of the input signal (speech, popular music, etc.), the attack time of a compressor generally lies in the range from 0.5 to 5 ms. The *release time* of the compressor is the time it takes the circuit to return to the settings that existed before the rise in amplitude occurred. Contrary to the attack time, the release time is usually of the order of seconds. If it is made too short, the compressor's attenuating action may cause interference with the lowest components in the frequency spectrum. On the other hand, too long a release time (10-15 s) is also undesirable as this will give rise to an unrealistic and unpleasant effect caused by the output sound remaining com-

pletely muted long after the increase in input signal amplitude. In practice, the release time of a compressor will need to be adapted to meet the demand of the particular input signal; speech generally requires a longer release time than music. Some compressors have a provision for the setting of the release time, but the one proposed here is an auto-ranging type, that is, it arranges for the release time to change automatically with the instantaneous amplitude of the input signal.

Figure 1 shows the circuit diagram of this compressor. Despite its simplicity, the design responds adequately to a good number of contradicting requirements. As to its dynamic characteristics, an input signal change from 25 mV<sub>pp</sub> to 20 V<sub>pp</sub> ( $\approx 58$  dB) is compressed into an output signal change from 1.5 V<sub>pp</sub> to 3.4 V<sub>pp</sub> ( $\approx 7.1$  dB). For a less extreme signal change, e.g., from 25 mV<sub>pp</sub> to 2.5 V<sub>pp</sub>

#### Measurement values:

A = 0 V  
B = +4.5 V  
C = 6 mA  
D = 3.9 V

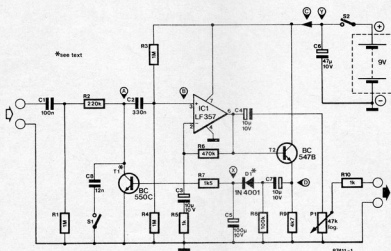
All values are typical and within 10%.

All voltages measured with respect to ground with a DMM ( $Z_{in} = 1M\Omega$ ).

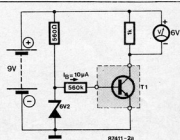
( $\approx 40$  dB), the compressed output signal changes from 1.5 V<sub>pp</sub> to 2.25 V<sub>pp</sub> ( $\approx 3.5$  dB). The circuit has an extended frequency response from about 20 Hz to 40 kHz nominally, thanks to the use of a fast opamp, the Type LF357 (IC1), which is set up here to provide an amplification of about 471  $[(R_6 + R_3)/R_5]$ . Capacitor C<sub>3</sub> blocks the direct voltage at the inverting input of IC1, and with R5 sets the low-frequency roll-off of the opamp alone at about 16 Hz.

Resistors R<sub>3</sub> and R<sub>4</sub> bias the non-inverting input of the opamp—and hence its output—at half the supply voltage, ensuring optimum linearity. Capacitor C<sub>2</sub> feeds the input signal to the opamp while blocking the bias voltage at pin 3. Its value is not critical, but it has some effect on the low-frequency response of the compressor. The attenuator section in this circuit is essentially composed of R<sub>2</sub> and T<sub>1</sub>. The collector of this transistor is held at 0 V with the aid of R<sub>1</sub> and R<sub>2</sub>. In this way, T<sub>1</sub> is always operated in its saturation region, and its collector-emitter junction acts as a variable resistance controlled with the current fed to the base. The higher this current, the lower the c-e resistance, and the higher the instantaneous attenuation of the signal fed to IC1. The controlling rectifier is composed of D<sub>1</sub>-C<sub>5</sub>-R<sub>7</sub>. Transistor T<sub>2</sub> functions to provide the charge current for C<sub>5</sub> so as to avoid distortion otherwise incurred by too heavily loading the IC1 output. The rectified voltage across C<sub>5</sub> is a direct measure of the output signal amplitude, and forward-biases the base of T<sub>1</sub>, which regulates the attenuation as dis-

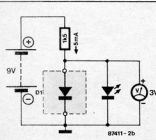
1



2a



b





cussed. The use of a diode with a low internal resistance,  $D_1$ , and a buffer,  $T_2$ , ensures fast charging and slow discharging of  $C_5$ , and thus a short attack time and a long release time, respectively. As  $C_5$  is discharged via  $R_7$  and the base resistance of  $T_1$ , the release time of the compressor is the product of the value of these three components. When the base bias is reduced, the base resistance of  $T_1$  increases, lengthening the release time. This is a most welcome feature, especially with speech signals. The output of the opamp is fed

to  $C_4$ - $P$ - $R_{10}$ , which provide DC insulation and level adjustment. Two compressors are readily combined to make a stereo version by feeding them from a common battery and connecting points X and points Y (never X to Y!). In this case,  $T_1$  and  $D_1$  in both compressors must be matched types to ensure proper operation. Figure 2 shows two simple test circuits for selecting transistors and diodes with matching DC characteristics. The basic method is to start with noting the voltmeter reading for a particular device, and then find a

matching type from an available lot by inserting devices until one is found that gives the previously noted test voltage. In the diode test circuit, the LED lights to indicate the absence or reverse connection of a diode under test.

Provision has been made to use the circuit as a noise suppressor. Referring to Fig. 1, closing  $S_1$  connects  $C_5$  across the regulator transistor to form a low-pass filter in conjunction with  $R_1$  and  $R_2$ . The cut-off frequency of this LPF is a function of the current sent into the base of  $T_1$ . The overall effect thus

obtained is an effective elimination of noise from quiet passages in the programme. For louder passages, the suppression of noise is not so important, as it is then virtually inaudible. Finally, when using this compressor, make sure that your amplifier has ample cooling provision, because it may well be continuously operated at the top of its power rating. For the same reason, check whether the loudspeakers can handle the available power.

SV

## 63

## DISCRETE DAC

A digital-to-analogue converter (DAC) that is easy to build from a handful of readily available parts. The 8-bit digital input for the circuit is applied to resistors  $R_{17}$ - $R_{24}$  incl., each of which drives an associated current source composed of two series-connected diodes, a transistor and a current defining resistor fed from the positive supply rail. A logic high level at the input causes the relevant current source to be switched on, a logic low level switches it off. The sum of currents from  $T_1$ - $T_8$  incl. is arranged to pass through preset  $P_1$ , which thus drops a voltage  $U_o$  in accordance with

the magnitude of the 8-bit word written to the circuit.

The current supplied by each current source is about  $700/R_x$  [mA], where  $R_x$  is the value of the associated resistor between the emitter and the +V rail. In order to ensure satisfactory linearity of the analogue output voltage, resistors  $R_1$ - $R_8$  incl. must be dimensioned to obtain a current ratio of 1:2 between any two adjacent sources. In practice, it is wise to first apply a logic high voltage to the MSB (most significant bit) input of the circuit, leaving the remaining inputs low, and measure  $U_o$  with the aid of a good-quality

voltmeter. Next, drive  $D_8$  high and all other inputs low, and make sure that  $U_o$  drops to half the previously obtained level by dimensioning  $R_7$  as required. The other current determining resistors are similarly established; the value of  $R_1$ - $R_8$  incl. that gives the correct level of  $U_o$  is obtained by making suitable combinations of series and/or parallel connected high stability resistors. Alternatively, it is possible to use multi-turn presets. As all resistors  $R_1$ - $R_8$  incl. must be dimensioned starting from a particular value of  $R_8$ , this resistor must first be calculated considering that the

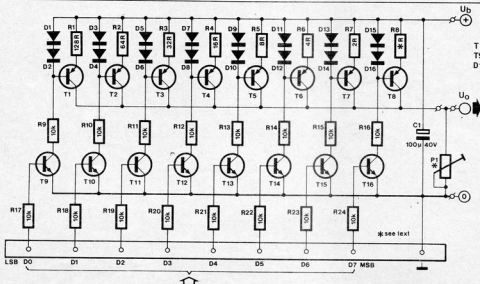
output linearity of the circuit is affected unless

$$1.4P_1/R_8 < (U_o) - 2$$

In practice, the maximum feasible level of  $U_o$  is about  $\frac{1}{2}U_{B1}$  [V] with only MSB high, and this level should be observed in the dimensioning of  $R_8$  and the setting of  $P_1$ .

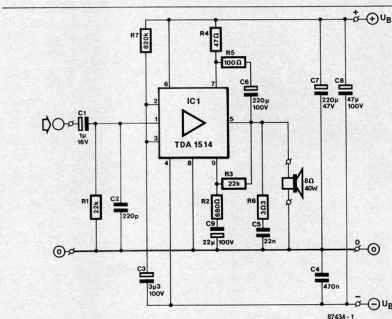
Although this 8-bit DAC should be sufficiently accurate for most practical applications, it is of course possible to opt for a greater or smaller number of current sources with a corresponding increase or decrease in the available resolution of  $U_o$ .

AR



T1...T8 = BC557B  
T9...T16 = BC547B  
D1...D16 = 1N4148  
87435

To answer the need for a compact amplifier that is capable of satisfactory operation when driven from a compact disc player, Philips have developed the Type TDA1514 AF amplifier chip, which is remarkable for its excellent specifications, ruggedness and output power. The device is housed in a 9-pin SIL POWER enclosure which has a thermal resistance of less than 1.5 K/W, so that the heatsink required must have a thermal resistance of no more than 3.8 K/W if the chip is operated at its maximum dissipation of 19 W ( $U_b = \pm 27.5$  V,  $T_a = 50^\circ\text{C}$ ). The circuit diagram shows that very few components are needed to make this high-performance amplifier. The power supply to feed the chip must be capable of delivering a current of at least 3 A; the quiescent current demand of the amplifier as shown is about 60 mA. The supply voltage should not exceed  $\pm 27.5$  V. Although this project is not supported by a ready-made printed circuit board, you should not experience too much difficulty in constructing the amplifier if it is built on a piece of Veroboard. Make sure, however, that the tracks and connections to the supply and output terminals are as short as possible, and use double tracks where this is necessary. In this context, it is advisable to fit decoupling capacitors  $C_1$  and  $C_2$  as close as possible to the chip supply pins. Resistors  $R_2$  and  $R_3$  deter-



mine the amplifier's closed loop voltage gain, which has a range of 20 to 46 dB. Finally, some measurement data obtained with a prototype of the amplifier:

$P_o$  at  $D_{tot} = -60$  dB;

$U_b = \pm 27.5$  V;  $R_L = 8\Omega$ : 40 W

S/N at  $P_o = 50$  mW: 82 dB

Supply ripple rejection

at  $f = 100$  Hz: 72 dB

Harmonic distortion at

$P_o = 32$  W: -85 dB

Intermodulation distortion

at  $P_o = 32$  W: -80 dB

3 dB bandwidth at  $D_{tot} =$

-60 dB: 20-25 000 Hz

Slew rate: 15 V/ $\mu$ s

Table

$P_o = 10$  W<sub>rms</sub>

Total harmonic distortion level

Order no.	1	2	3	4	5	6
100 Hz	-79	-84	-84	-	-	-
1 kHz	-69	-82	-78	-86	-82	-
10 kHz	-55	-76	-65	x	x	x

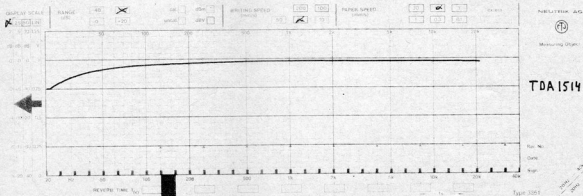
-: below analyser's noise floor (-87 dB)

x: analyser unsuitable for measurement.

The gain vs frequency curve and the harmonic distortion table show that this amplifier

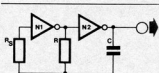
provides very good sound reproduction at a considerable output power level.

ST



When frequency stability is not of prime importance, a simple, yet reliable, digital clock oscillator can be made with the aid of relatively few components. High-speed CMOS (HCU/HCT) inverters or gates with an inverter function are eminently suitable to make such oscillators, thanks to their low power consumption, good output signal definition and extensive frequency range.

The circuit as shown uses two inverters in a 74HCT04 or



N1, N2 = 1/3 IC1 = 74HCT04, 74HCU04

87437

74HCU04. The basic design equations are

for HCU:  $f = 1/T$ ;  $T = 2.2RC$ ;  
 $3V < V_{cc} < 6V$ ;  $I_c = 13 \text{ mA}$

for HCT:  $f = 1/T$ ;  $T = 2.4RC$ ;

$4.5V < V_{cc} < 5.5V$ ;  $I_c = 2.25 \text{ mA}$

$R_s \geq 2R$ ;  $IK\Omega \leq R \leq 1M\Omega$ ;  $C \geq 10 \text{ nF}$ .

With  $R_s$  and  $R$  calculated for a given frequency and value of  $C$ ,

both resistors can be realized as presets to enable precise setting of the output frequency and the duty factor. Do not forget, however, to fit small series resistors in series with the presets, in observance of the minimum values for  $R$  and  $R_s$  as given in the design equations. The values quoted for  $I_c$  are only valid if the inputs of the remaining gates are grounded.

Source: *Philips CMOS Designers Guide*, January 1986, p. 105 ff. St

by R Shankar

Switching audio signals digitally could be done with the aid of CMOS analogue switches or multiplexers. Simple as this may seem, there is, however, an inevitable loss in the quality of the sound due to the noisy nature of CMOS switches. Furthermore, the high on-resistance of these devices together with the large parasitic capacitances generally present

in CMOS circuits causes a high susceptibility to crosstalk. The circuit given here is a novel way of selecting one out of ten audio signals digitally without any of the foregoing drawbacks.

As shown in the circuit diagram, the ten input signals numbered 1-10 are applied to the bases of transistors  $T_1$ - $T_{10}$  via capacitors  $C_1$ - $C_{10}$  respectively. The bias voltages for the

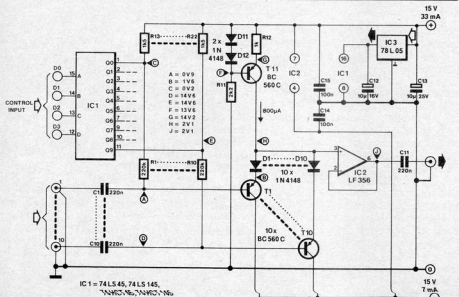
transistors are obtained with the aid of  $R_1$ - $R_{10}$ . Depending on the binary state applied to  $IC_1$ , one of its outputs  $Q_0$ - $Q_9$  goes low. For example, if the input code is 0010  $Q_2$  goes low, pulling the base of  $T_3$  to 0 V, while the bases of all other transistors are raised to nearly +15 V. Therefore,  $T_3$  works as an emitter follower while the other transistors are effectively reverse

biased. The output rail of the transistor array is connected to voltage follower  $IC_2$ , which provides the output signal of the digital audio selector.

Voltage regulator  $IC_3$  is required only if a +5 V rail is not available. If the number of channels required for a particular application is less than 10, the relevant components can be omitted. If a mute facility is required, simply short one input to ground to silence the output on selection of the corresponding channel.

This circuit can handle input signals up to 4 V<sub>rms</sub>. The total distortion does not exceed 0.01% for frequencies up to 20 kHz. The crosstalk incurred in this circuit is less than -80 dB. This value can be attained by paying due attention to the layout of the practical circuit, the decoupling of the supply lines (fit  $C_{14}$  and  $C_{15}$  direct to the relevant pins of the opamp), and the use of good quality components.

The measuring values indicated in the circuit diagram were obtained in a prototype. All voltages are measured with respect to ground with the aid of a DMM ( $Z_{in} = 1M\Omega$ ). The channel selectivity was number 1.



IC1 = 74LS45, 74LS145,  
74HCT04, 74HCU04

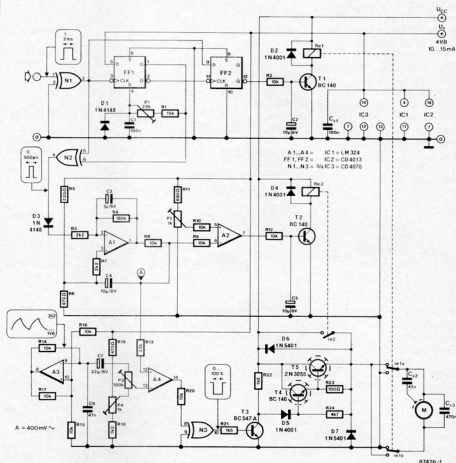
87443

by P Techer

The speed and direction of rotation of a motor in a radio controlled model aeroplane or boat is generally controlled by pulse width modulation of the supply voltage to the motor driver stage.

In the present circuit, shown in Fig. 1, bistable FF<sub>1</sub> is set up rather unconventionally to function as a monostable multivibrator, whose period is set with R<sub>1</sub>-C<sub>1</sub>-P<sub>1</sub>. This period determines the toggle point at which the motor's direction of rotation is reversed. Output Q of FF<sub>2</sub> goes high when the pulse at the D input (PWM signal) is shorter than that at the CLK input (signal from FF<sub>1</sub>). This causes T<sub>1</sub> to actuate Re<sub>1</sub>, so that the motor direction is reversed. The PWM control signal applied to the circuit is also fed to N<sub>2</sub>, whose output pulse width is the difference between that of the input signal and that from FF<sub>1</sub>. The pulse width at the output of N<sub>2</sub> therefore increases as the relevant control handle on the transmitter is moved further towards either extreme, and is maximum when the handle is in the central position. The output of N<sub>2</sub> is integrated by A<sub>1</sub> to obtain an output voltage proportional to the pulse width. A<sub>4</sub> compares this output voltage with the triangular signal at the wiper of P<sub>1</sub>, so that a variable duty factor signal is obtained for driving the power output stage comprised of T<sub>4</sub>-T<sub>5</sub>. Meanwhile, A<sub>2</sub> compares the proportional voltage from A<sub>1</sub> to the level set with P<sub>2</sub>. When the output of A<sub>1</sub> is lower than the threshold, i.e., when the motor speed exceeds the preset level, T<sub>2</sub> activates Re<sub>2</sub>. This causes the collector-emitter junction of series regulator T<sub>3</sub> to be bypassed by the relay contact, and so enables the motor to run at full speed, because the forward drop across T<sub>3</sub> is eliminated. The frequency of the triangular signal from A<sub>3</sub> is of the order of 2 kHz, which is suitable for most motors. Capacitor C<sub>6</sub> may be increased to lower the frequency for non-standard

1

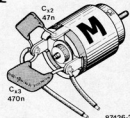


motors. Conversely, if the frequency is increased, care should be taken to observe the maximum switching speed of T<sub>3</sub>, which is a commonly available, but relatively slow power transistor. Presets P<sub>1</sub> and P<sub>2</sub> determine the limits of the inoperative range of the handle, i.e., when the motor speed exceeds the preset level, T<sub>2</sub> activates Re<sub>2</sub>. This causes the collector-emitter junction of series regulator T<sub>3</sub> to be bypassed by the relay contact, and so enables the motor to run at full speed, because the forward drop across T<sub>3</sub> is eliminated. The frequency of the triangular signal from A<sub>3</sub> is of the order of 2 kHz, which is suitable for most motors. Capacitor C<sub>6</sub> may be increased to lower the frequency for non-standard

sufficiently large control range for the handle, and also to avoid the risk of Re<sub>2</sub> clattering or being blocked.

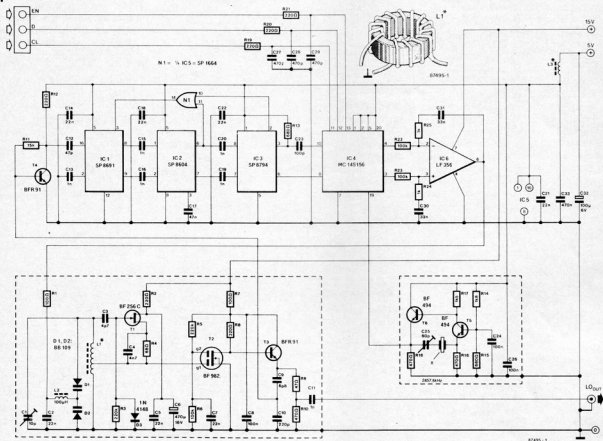
Be sure to fit the 470nF capacitor across the motor terminals, and the 47nF capacitor between one of these and the motor body—see Fig. 2. The coil voltage of the relays should be equal to the voltage for the battery that powers the motor, while the contacts must be capable of handling the current demand of the motor. Transistors T<sub>4</sub> and T<sub>5</sub> should be fitted with a heatsink. Note that although the Type 2N3055 can handle currents up to 10 A, it may be a good idea to fit two in parallel with 0R1 emitter resistors for equal current distribution when heavy loads are to be controlled. The cur-

2



rent rating of D<sub>5</sub> and D<sub>7</sub> must also be observed: for the stated 1N5401s, I<sub>S(max)</sub> = 3 A, and two may have to be connected in parallel when this current is approached. Finally, U<sub>+</sub> is the model's battery voltage (4.8 V), and +U<sub>cc</sub> is the supply voltage for the motor.

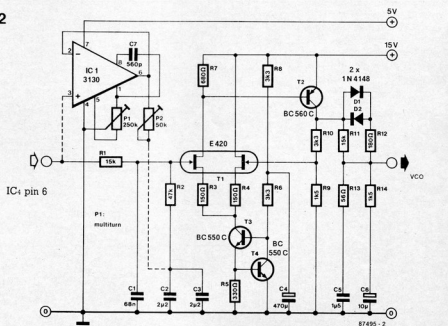
1



The synthesizer shown in Fig. 1 is computer controlled, and outputs a local oscillator signal (LO) between 48 and 78 MHz for driving the mixer in the SW receiver proposed on page 00. The circuit is based on the Type MC145156 synthesizer from Motorola. This IC is relatively inexpensive, and ensures good LO suppression in the receiver when used in combination with a good mixer. Also of interest is its serial control input, which enables the output frequency to be programmed from a computer.

The internal reference frequency, 1200 Hz, is obtained by dividing the signal from oscillator T<sub>5</sub>-T<sub>6</sub> by 2048. The DAC connected to the output of the first LO gives a resolution of 1200/255 = 5 Hz. The divider composed of IC<sub>1</sub>, IC<sub>2</sub>, IC<sub>3</sub> and N<sub>1</sub> has a prescale factor of

2



[illegible]

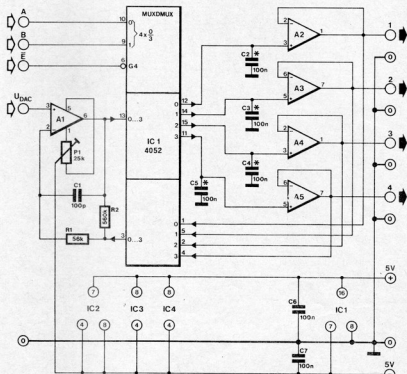
the control word is complete, the enable signal is briefly made high to transfer the data from the shift register to the programmable dividers. The squelch is then enabled to suppress locking and tuning noises. The construction of this synthesizer requires some experi-

月

## 69

## 4-WAY DAC EXTENSION

For optimum performance, C<sub>2</sub>-C<sub>3</sub> should be low leakage capacitors, e.g. multilayer MKT, and the input current to A<sub>2</sub>-A<sub>3</sub>



A1 = IC 2 = TLC 271  
A2, A3 = IC 3 = TLC 272  
A4, A5 = IC 4 = TLC 272

\* see text

87453

should remain low. The latter condition is satisfied by using opamps with FET inputs (typical bias current: 1 pA). Only A<sub>1</sub> requires an offset compensation since feedback is provided via the lower multiplexer

in IC<sub>1</sub>. The E (enable) input serves to disable IC<sub>1</sub> during switchover to another channel. R<sub>2</sub> then gives A<sub>1</sub> unity gain to prevent the - input being left open. When a Type HCT4052 is used

in the IC<sub>1</sub> position, standard TTL levels can be used to drive inputs A, B and E. A "normal" CMOS 4052 requires 5K6 pull-up resistors to be fitted on these inputs, but only if TTL signals are used to drive the extension.

The current consumption of the circuit is less than 10 mA. U<sub>DAC</sub> should be between -3.5 V and +3.5 V.

Th

## 70

# VARIABLE WIEN BRIDGE OSCILLATOR

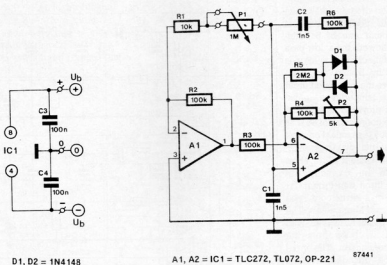
A Wien bridge oscillator can be made variable by using two frequency determining parts that are varied simultaneously at high tracking accuracy. High-quality tracking potentiometers or variable capacitors are, however, expensive and difficult to obtain. To avoid having to use such a component, this oscillator was designed to operate with a single potentiometer. The output frequency,  $f_o$ , is calculated from

$$f_o = 1 / (2\pi RC\sqrt{\phi})$$

where  $R = R_2 = R_3 = R_4 = R_5$ ,  $C = C_1 = C_2$ , and  $\phi = (P_1 + R_1)/R$ . Preset P<sub>2</sub> allows adjusting the overall amplification such that the output signal has a reasonably stable amplitude (3.5 V<sub>pp</sub> max.) over the entire frequency range.

The stated components allow the frequency to be adjusted between 350 Hz and 3.5 kHz. Other frequency ranges are readily defined with the aid of the above formula, although it should be noted that the upper

1



D1, D2 = 1N4148

A1, A2 = IC1 = TLC272, TL072, OP-221

87441

frequency limit is determined mainly by the gain-bandwidth product of the opamps Type OP-221 and TLC272. The current consumption of the oscillator depends on the type of opamp

used. The following values were measured: OP-221: 0.5 mA; TLC272: 2 mA; TL072: 2 mA. The construction of the oscillator should present very few problems since a ready-made

circuit board is available through our Readers Services. Sv

(PMI Application)

### Parts list

Resistors ( $\pm 5\%$ ):

- R<sub>1</sub> = 10K
- R<sub>2</sub>, R<sub>3</sub>, R<sub>4</sub>, R<sub>5</sub> = 100K
- R<sub>6</sub> = 2M2
- P<sub>1</sub> = 1M0 linear potentiometer
- P<sub>2</sub> = 5K0 preset

Capacitors:

- C<sub>1</sub>, C<sub>2</sub> = 1n5
- C<sub>3</sub>, C<sub>4</sub> = 100n

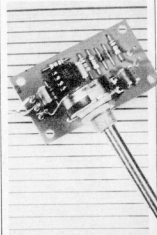
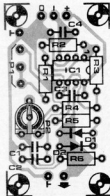
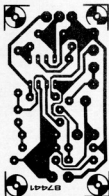
Semiconductors:

- D<sub>1</sub>, D<sub>2</sub> = 1N4148
- IC<sub>1</sub> = TLC272 or TL072 or OP-221

Miscellaneous:

- PCB Type 87441 (see Readers Services).

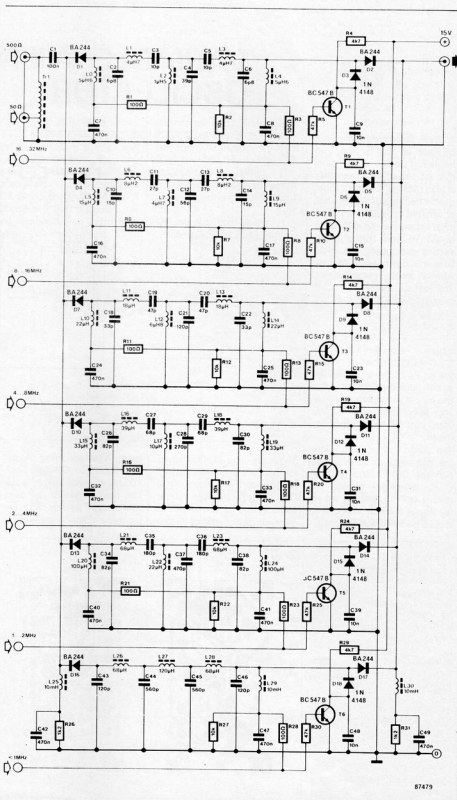
2



In many older types of SW receiver, intermodulation in the mixer was generally avoided by including a tuneable, often automatically tracking, pre-selector. In a computer-controlled preselector, the use of varactor diodes for tuning the inductors often leads to considerable intermodulation distortion. A different approach is therefore used in this design.

The circuit diagram shows the use of PIN diodes Type BA244 for selecting one of 5 band-pass filters followed by a low-pass section. Selection of a filter is effected by having the computer drive the associated input high. An impedance transformer is provided at the input to enable connection of 50  $\Omega$  as well as 500  $\Omega$  aerials. For most purposes, the 500  $\Omega$  input is preferable, since it allows short aerials to be correctly terminated. Input transformer T<sub>1</sub> is wound on a ferrite core Type FT37-75 from Micrometals. The total number of turns is 19, with a tap at 2½ turns from the ground connection. The input should be provided with an overvoltage protection if the aerial is a large, outside mounted, array.

B





This circuit is used for optimum regulation of the flow of hot water in a central heating system. It measures the water temperature, and arranges for a particular valve or pump in the system to be switched on to achieve a user-defined temperature distribution in the home. Residual heat in the central heating system can thus be used to lower the cost of fuel. Fig. 1 shows that water in temperature range **I** can be used for the central heating and the storage vessel, while that in range **II** is also suitable for directing to the boiler. In most cases, it is not recommended to re-use water with a temperature below 30 °C. The circuit arranges for an alarm to be activated when the water temperature falls below 5 °C, or exceeds 95 °C.

The circuit diagram of the central heating control appears in Fig. 2. Relays Re<sub>1</sub> and Re<sub>5</sub> are activated upon measuring the maximum and minimum permissible temperature, respectively. The temperature sensor is a Type LM35, which has a scale factor of +10 mV/°C. Its output voltage is amplified in A<sub>1</sub> and fed to the non-inverting inputs of comparators A<sub>2</sub>-A<sub>4</sub>. The presets at the inverting input of each of these is used to set the toggle voltage, i.e., the temperature at which the relevant relay

is switched on or off. The relay drivers are open-collector power buffers with built-in freewheeling diodes to afford protection against inductive surges. The use of the Type ULN2003 makes it possible to use relays with a coil voltage of up to 50 V without the need for additional interfacing.

Each temperature setting has a hysteresis of about 2 °C. Transistors T<sub>1</sub>-T<sub>3</sub> serve to disable the previously energized pump or valve upon detecting a water temperature that falls within another, predefined, range. In

this manner, only one relay is activated at a time.

It stands to reason that the temperature sensor, IC<sub>1</sub>, must be mounted such that it is in thermal contact with the water in the heating system. Make sure that the device is well-insulated, and that it does not cause leakage.

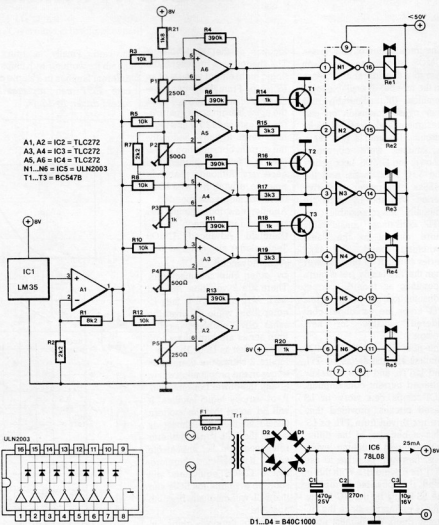
The temperature range settings for the presets are shown opposite.

Relay	Preset	Temperature range
1	P <sub>1</sub>	93-103 °C (upper limit alarm)
2	P <sub>2</sub>	77-93 °C
3	P <sub>3</sub>	33-77 °C
4	P <sub>4</sub>	11-33 °C
5	P <sub>5</sub>	5-11 °C (lower limit alarm)

(hysteresis on all toggle points: 2 °C).

SR

2

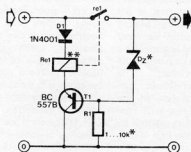


by R Kambach

Any diode-based circuit that protects against reversal of the supply polarity introduces a certain voltage drop. Also, when relatively high currents are involved, the choice of a suitable diode, and its dissipation, may become problematic.

This circuit utilizes a relay contact to break the positive supply line when the input voltage has

the wrong polarity. The coil voltage of the relay may be lower than the input voltage, because  $R_{e1}$  is activated within a few milliseconds, and then receives the correct coil voltage via  $T_1$ - $D_1$ . Since the hold voltage of a relay is generally lower than the actuation voltage,  $D_2$  can be dimensioned such that the relay operates reliably with a minimum of zener current taken from the supply.  $D$



The introduction of new, faster, CMOS techniques has given rise to a considerable increase in the number of available logic families. Understandably, this may cause confusion on part designers and users of logic circuits. Up until a few years, 3 families were commonly known: the CMOS 4xxx series; the TTL 74xx series; and the 74LSxx low-power Schottky series. TTL and LS chips are mutually interchangeable, but TTL consumes considerably more current at the same switching speed. The 4xxx series is about 10 times slower than the TTL family, but is more economic as regards current consumption. In many cases, TTL chips are no longer considered suitable for new design.

The new HC and HCT CMOS families are just as fast as TTL and LS/TTL, and have a greatly reduced current consumption. HCT chips can work in LS based circuits, provided they are not driven from TTL or LS. This is because of the differently defined switching levels. It is, however, possible to use HCT for driving HC. With this in mind, it is possible to replace the LS family by the HC family. This is preferable since the HC family offers the highest noise immunity.

Figure 1 shows the current consumption of a HCMOS gate as a

function of the input voltage. The shaded area represents the (logic high) output voltage of an LS chip. From this, two conclusions can be drawn. Firstly, the noise margin is very narrow: the HC gate sees 2.7 V as a logic high level already. Secondly, the current consumption of the gate is a few mA higher than necessary. Although usable in practice, driving HC with LS is, therefore, not recommended.

Another new logic family was recently introduced: FACT (Fairchild Advanced CMOS Technology), also referred to as ACL (Advanced CMOS Logic) by other chip manufacturers. There are 2 versions: AC and ACT. ACT, like HCT, is fully LS compatible, while AC gives the same drive problems as HC.

Both series are typically 2 to 3 times as fast as LS or HC. Figure 2 shows the correlation between the propagation delay,  $t_p$ , and the power consumption,  $P$ , of various logic families. It will be noted that the modern CMOS families are almost as fast as the ECL series, hitherto renowned for its unbeatable speed. It is expected, therefore, that a CMOS equivalent will soon be available for ECL, and that ECL will gradually become obsolete.

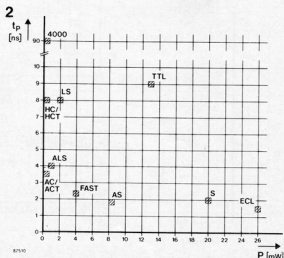
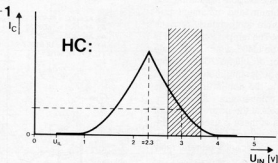
Replacing bipolar chips in existing circuits with CMOS types is not very useful if relatively high frequencies are

involved. Finally, a rule of thumb for working with chips of different families in a single circuit: HCT can replace LS, unless driven by LS.  $W$

For further reading:

RCA CMOS Databook

Fairchild FACT Logic Data Book

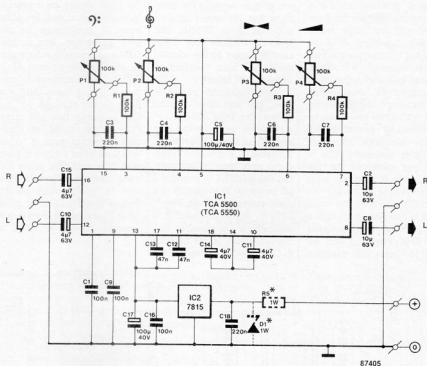




This simple, one-chip, stereo preamplifier is ideal for building into an existing AF power amplifier. It is based on a recently introduced integrated circuit, the Type TCA5500 or TCA6550 from Motorola. This double AF amplifier chip with inputs for balance, volume, and bass and treble controls forms a sound basis for a good quality preamplifier with a minimum of components. The onset points for the bass and treble controls are defined with  $C_3$  and  $C_4$  respectively. All (mono) potentiometers are best fitted direct onto the circuit board to make for simple mounting into a cabinet, and also to prevent hum and noise being picked up in the wiring that would otherwise be required.

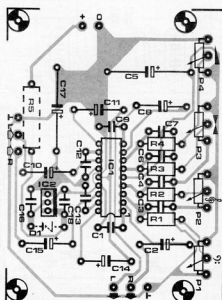
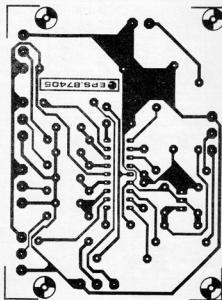
The preamplifier has a current consumption of 35 mA, of which 5 mA is drawn by voltage regulator  $IC_2$ . Zenerdiode  $D_1$  and power resistor  $R_5$  should be added if the positive supply voltage available in the power amplifier is more than about 30 V.

Fe



\* see text

87405



## Parts list

Resistors ( $\pm 5\%$ ):

$R_1 \dots R_4$  incl. = 100K

$R_5$  = see text

$P_1 \dots P_4$  incl. = 100K linear potentiometer

Capacitors:

$C_1; C_2; C_{16}$  = 100n

$C_3; C_4$  = 10 $\mu$ ; 63 V; radial

$C_5; C_6; C_7; C_{18}$  = 220n

$C_8; C_{17}$  = 100 $\mu$ ; 40 V; radial

$C_{19}; C_{15}$  = 4 $\mu$ ; 63 V; radial

$C_{11}; C_{14}$  = 4 $\mu$ ; 40 V; radial

$C_{12}; C_{13}$  = 47n

Semiconductors:

$D_1$  = zener diode 27 V; 1 W

(see text)

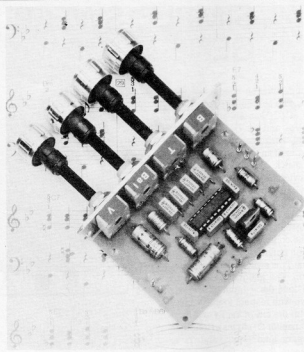
$IC_1$  = TCA5550 or TCA5550

(Motorola)

$IC_2$  = 7815

Miscellaneous:

PCB Type 87405 (available through the Readers Services).



## Specifications of the preamplifier:

Distortion:  $\leq 0.1\%$  at nominal output level.

Channel separation:  $\geq 45$  dB.

Supply voltage: 8.8-18 V.

Tone control range: 14 dB.

Volume control range:  $\geq 75$  dB.

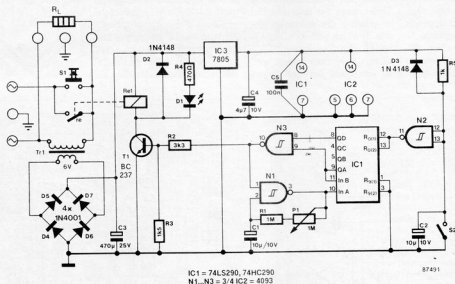
Maximum input voltage: 100 mV.

Amplification: 10.

Low output impedance.

# 77

## TIMER FOR SOLDERING IRON



## By K Feigl

It often happens that the soldering iron is left switched on, but unattended and out of its stand. Evidently, this is a waste of energy, and an unnecessary fire hazard at the same time. This circuit arranges for the soldering iron to be switched off automatically

when it is out of its holder for more than about 20 seconds. The output frequency of clock oscillator  $N_1$  is adjustable with  $P_1$ . Decimal counter  $IC_1$  divides the clock by 10. When both  $Q_A$  and  $Q_D$  are high, i.e., when counter state 9 is reached,  $N_3$  turns off  $T_1$ . Hence both the soldering iron and the timer are switched off because  $R_{e1}$  is de-

activated. Pressing key  $S_1$  causes the circuit to become operative again. Capacitor  $C_2$  is not yet charged, so that  $IC_1$  is reset by  $N_2$ . Gate  $N_3$  is therefore driven with two logic low levels, so that  $T_1$  energizes  $R_{e1}$ . The mains voltage is now applied to the soldering iron (= load  $R_L$ ) and  $T_1$  via contact re.

Switch  $S_2$  should be closed when the soldering iron is in its holder or stand. This causes the counter to remain reset, and hence the relay to remain energized, until  $S_2$  is opened. The above timing sequence is then started, and can be interrupted only by placing the iron in the stand within 20 seconds. W

The sweep generator is an indispensable piece of measuring equipment for testing the frequency response of AF amplifiers, filters, and loudspeaker systems. At the heart of this design is the well-known Type XR2206 function generator chip from EXAR. It is seen to the right on the circuit diagram, in a standard application with 3 capacitors and a rotary switch for selecting the frequency range, and a potentiometer,  $P_5$ , for adjusting the amplitude of the output signal. The signal frequency is a function of the current drawn from pin 7 on the XR2206:

$$f_0 = 3201/C \text{ [Hz]}$$

where  $I$  is in milli-amperes, and  $C$  is in micro-farads. It should be noted that pin 7 is internally kept at 3 V, which is available at pin 10 also.

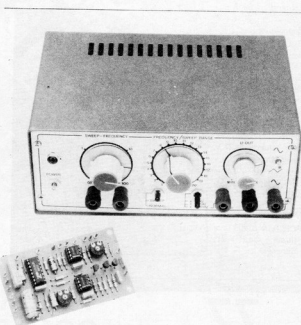
The left-hand part of the circuit comprises the sawtooth generator,  $IC_1$ , and a buffer,  $IC_2$ . The former is set up as an integrator, whose sweep period depends on the voltage at terminal C. Potentiometer  $P_1$  enables setting the sweep period between 0.01 and 10 seconds; the maxi-

mum duration is adjusted with  $P_4$ . The sawtooth voltage at pin 6 of  $IC_1$  has an amplitude of  $5V_{PP}$ , and can be used to drive the horizontal deflection (X) input of an oscilloscope via terminal K. The amplitude of the sawtooth voltage is determined by the zener voltage of  $D_1$  and the base-emitter voltage of  $T_1$ , which is briefly turned off when the output of  $IC_1$  exceeds 5 V. The collector of this transistor is then pulled to ground via  $R_3$ , so that  $T_1$  is switched into conduction. The integrator is reset by making the - input of  $IC_1$  positive with respect to the + input with the aid of  $T_2$ ,  $R_5$  and  $R_6$ .

Capacitor  $C_1$  serves to lengthen the on-time for  $T_1$  and  $T_2$  to ensure that the flyback of the sawtooth is finished.

Potentiometer  $P_1$  is a voltage divider to define the sawtooth amplitude, and hence the sweep range, while  $S_1$  makes it possible to turn off the sweep function (position F).

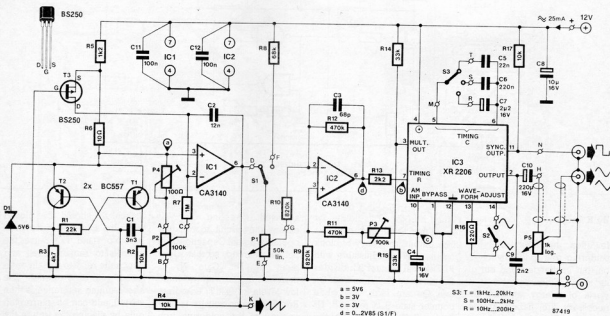
Opamp  $IC_2$  is configured as a buffer stage for inverting and attenuating the sawtooth voltage, to which a direct voltage is added also. The output of  $IC_2$  carries a sawtooth voltage with an amplitude between 0 and

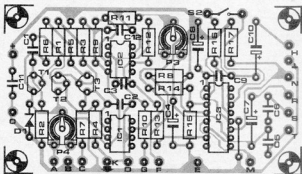
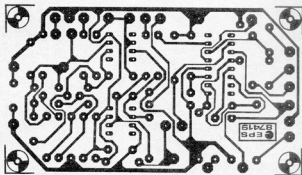
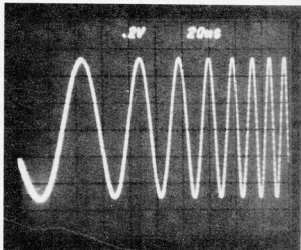


2.85 V, or a direct voltage between the same limits when  $S_1$  is set to position F. Bearing in mind that the reference voltage of  $IC_2$  is 3 V, the current through  $R_{13}$ , and hence the output frequency, can be varied by a factor 20, which is the maximum attainable deviation factor in all

3 frequency ranges. The frequency scale can be calibrated with the aid of  $P_5$ .

TW





## Parts list

### Resistors ( $\pm 5\%$ ):

$R_1 = 22K$   
 $R_2, R_4, R_{17} = 10K$   
 $R_3 = 4K7$   
 $R_5 = 1K2$   
 $R_6 = 10R$   
 $R_7 = 1M0$   
 $R_8 = 68K$   
 $R_9, R_{10} = 820K$   
 $R_{11}, R_{12} = 470K$   
 $R_{13} = 2K2$   
 $R_{14}, R_{15} = 33K$   
 $R_{16} = 220R$   
 $P_1 = 50K$  linear potentiometer  
 $P_2 = 100K$  linear potentiometer  
 $P_3 = 100K$  preset  
 $P_4 = 100R$  preset  
 $P_5 = 1K0$  logarithmic potentiometer

### Capacitors:

$C_1 = 3n3$   
 $C_2 = 12n$   
 $C_3 = 68p$   
 $C_4 = 1\mu$ ; 16 V; radial  
 $C_5 = 22n$   
 $C_6 = 220n$   
 $C_7 = 2\mu2$ ; 16 V; radial  
 $C_8 = 10\mu$ ; 16 V; radial  
 $C_9 = 2n2$   
 $C_{10} = 220\mu$ ; 16 V; radial  
 $C_{11}, C_{12} = 100n$

### Semiconductors:

$D_1 =$  zener diode 5V6; 400 mW  
 $T_1, T_2 = BC557$   
 $T_3 = BS250^+$   
 $IC_1, IC_2 = CA3140$   
 $IC_3 = XR2206^+ +$

### Miscellaneous:

$S_1 =$  miniature SPDT switch.  
 $S_2 =$  miniature SPST switch.  
 $S_3 =$  1 pole, 3-way rotary switch.

PCB Type EPS87419 (available through the Readers Services).

<sup>+</sup> Available from Universal Semiconductor Devices Limited, Cricklewood Electronics Limited, or ElectroValue (28 St Judes Road, Englefield Green, Egham, Surrey TW20 0HB. Telephone: (0784) 33603; telex 264475).

<sup>\*</sup> Available from Cricklewood Electronics Limited.

This high quality phono pre-amplifier is based on the Type HA12017 integrated circuit from Hitachi. The principal technical data of this chip are summarized in Table 1. The circuit diagram, Fig. 1, shows that output off-set correction is provided by integrator IC2. The output signal of IC1 is first passed through low-pass filter R7-C9, then integrated in IC2-C10. The error signal is fed to the inverting input of amplifier IC1 via 47 k $\Omega$  resistor R6. The amplitude of this signal is

always such that the off-set voltage at the output of IC1 is virtually nought. The off-set correction used here enables the preamplifier to drive a power amplifier direct.

The correct capacitive termination of the pick-up cartridge can be selected with the aid of S1. The input impedance is 50 k $\Omega$ , but can be altered by redimensioning R2-R3. The output impedance of the preamplifier is 510  $\Omega$ , i.e., low enough for driving a relatively long cable. The RIAA equalization filter in

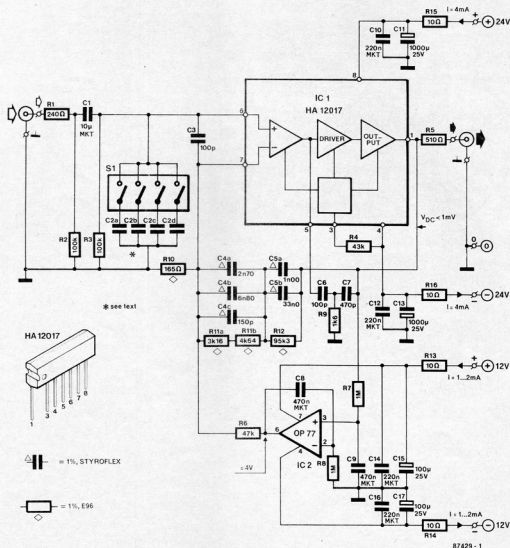
Table 1. HA12017 Low noise preamplifier

Features:

- Low noise:  $V_n(in) = 0.185 \mu V$  typ. (measured in IHF-A network,  $R_g = 43 \text{ k}\Omega$ , IEC RIAA).  $V_n = -95 \text{ dB}$  relative to  $V_o = 1 \text{ V}_{rms}$ .
- Wide dynamic range:  $V_i = 235 \text{ mV}_{rms}$  max. ( $V_{cc} = \pm 24 \text{ V}$ ,  $f = 1 \text{ kHz}$ ,  $THD = 0.1\%$ ,  $A_v = 100 \pm 40 \text{ dB}$ ).
- Low distortion:  $THD = 0.002\%$  typ. ( $f = 20\text{--}20\,000 \text{ Hz}$ ,  $V_o = 10 \text{ V}_{rms}$ , RIAA equalization).
- Supply ripple rejection:  $SVR(+V_{cc}) = 56 \text{ dB}$ ;  $SVR(-V_{cc}) = 45 \text{ dB}$  (typical values at  $f = 100 \text{ Hz}$  and  $R_g = 43 \text{ k}\Omega$ ).
- Maximum operating voltage:  $\pm 26 \text{ V}$ .
- Maximum power dissipation:  $500 \text{ mW}$  at  $T_a = 75^\circ\text{C}$ .

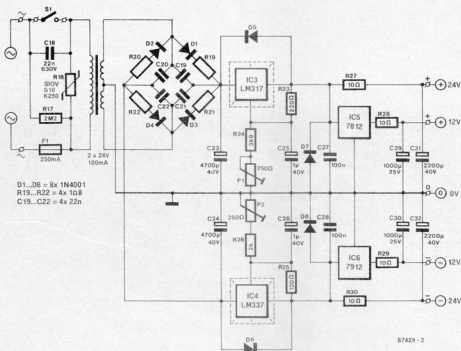
Note:  $R_g = R_4$  in this design.

1





2



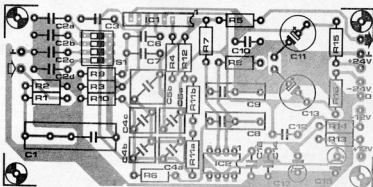
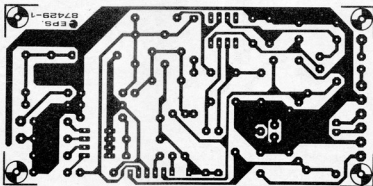
the negative feedback circuit of IC<sub>1</sub> is fairly complex, which was necessary to meet the required IEC specification (note the use of high stability capacitors and resistors).

The regulated power supply for the phono preamplifier is shown in Fig. 2. This is once again a relatively extensive circuit which, in combination with the low-pass filters on the  $\pm 24$  V lines to IC<sub>1</sub> and IC<sub>2</sub>, gives excellent suppression of RF signals, hum, rectification noise, and mains borne interference. Presets P<sub>1</sub> and P<sub>2</sub> serve to adjust the output voltage on the  $\pm 24$  V rails.

The printed-circuit boards for the preamplifier and the power supply are shown in Figs. 3 and 4 respectively. The correct values for R<sub>11</sub>, C<sub>4</sub> and C<sub>5</sub> are achieved by parallel and series connection. All four voltage regulators can be fitted onto a common heatsink if electrical insulation is provided. The accompanying photograph shows a suggested construction of the preamplifier.

It is strongly recommended to use good quality components for the volume adjustment and input source selection—consult the references given below. Sv

3



## Parts list

### Resistors ( $\pm 5\%$ ):

R1 = 240R  
R2; R3 = 100K  
R4 = 43K  
R5 = 510R  
R6 = 47K  
R7; R8 = 1M0  
R9 = 1K6  
R10 = 165RF  
R11 = 3K16F + 4K64F  
R12 = 95K3F  
R13...R16 incl.; R27...R30  
incl. = 10R  
R17 = 2M2  
R18 = varistor S10V S10K250  
(Siemens)  
R19...R22 incl. = 1R8  
R23 = 220R  
R24 = 3K9  
R25 = 120R  
R26 = 2K0  
P1; P2 = 250R preset

### Capacitors:

C1 = 10 $\mu$ ; MKT  
C2 = dimension to suit  
capacitive termination of  
cartridge.  
C3 = 100p; polystyrene  
C4 = 2n7F//6n8F//150p0F;  
styroflex  
C5 = 1n0F//33n0F; styroflex  
C6 = 100p styroflex  
C7 = 470p styroflex  
C8; C9 = 470n MKT  
C10; C12; C14; C16 = 220n MKT  
C11; C13; C25; C30 = 1000 $\mu$ ; 25 V;  
radial  
C15; C17 = 100 $\mu$ ; 25 V; radial  
C18 = 22n; 630 V  
C19...C22 incl. = 22n  
C23; C24 = 4700 $\mu$ ; 40 V; radial  
C25; C26 = 1 $\mu$ ; 40 V; radial  
C27; C28 = 100n  
C31; C32 = 2200 $\mu$ ; 40 V; radial

### Semiconductors:

D1...D8 incl. = 1N4001  
IC1 = HA12017 (Hitachi)<sup>†</sup>  
IC2 = OP-77 (Precision  
Monolithics Inc.)  
IC3 = LM317  
IC4 = LM337  
IC5 = 7812  
IC6 = 7912

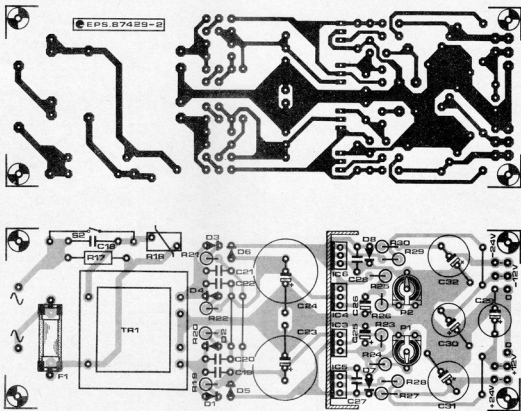
### Miscellaneous:

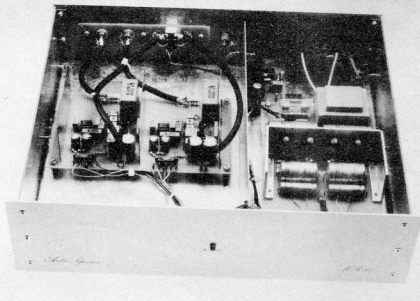
S1 = 4-way DIP switch block.  
S2 = SPST mains switch.  
F1 = 250 mA delayed action  
fuse with PCB mount holder.  
TR1 = 2x24 V; 100 mA mains  
transformer for PCB mount-  
ing.  
Heat-sink for IC3...IC6 incl.  
Insulating washers for  
IC3...IC6 incl.  
PCB Type 87429-1 and  
87429-2 (available through  
the Readers services).

Available from ElectroValue  
Ltd ■ 28 St Judes Road ■  
Englefield Green ■ Egham  
■ Surrey TW20 0HB. Tele-  
phone: (0784) 33603 ■  
Telex: 264475.

<sup>†</sup> Available from Cirkuit PLC  
■ Park Lane ■ Broxbourne  
■ Hertfordshire EN10 7NQ.  
Telephone: (0992) 444111 ■  
Telex: 22478. Stock number:  
61-170-12017.

*General note:* many special  
AF components for this pro-  
ject are available from  
Audiokits Precision Compo-  
nents ■ 6 Mill Close ■  
Borrowash ■ Derby DE7  
3GU. Telephone: (0332)  
674929.





#### References:

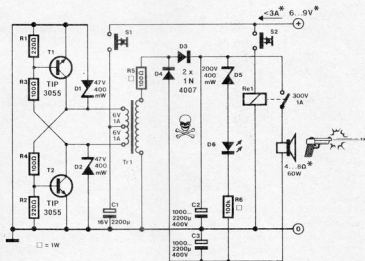
1. *Top of the range preamplifier*, Elektor Electronics, January 1987.
2. *Valve preamplifier*, Elektor Electronics, March 1987.
3. *Electronic potentiometers*, Elektor Electronics, April 1987.

# 80

## STARTING-PISTOL SIMULATOR

In this circuit, a discarded power loudspeaker serves to simulate the loud bang from a starting-pistol.

Power transistors  $T_1$ - $T_2$  and mains transformer  $Tr_1$  form a power oscillator, which can be started by pressing  $S_1$ . Zener-diodes  $D_1$ - $D_2$  protect  $T_1$ - $T_2$  against inductive voltage surges. The operating frequency of the oscillator depends on the core material of  $Tr_1$ , and the current through its 240 V winding. While  $S_1$  is kept actuated, the oscillation frequency is lowered from several kHz to about 50 Hz as the charge voltage across flash capacitors  $C_2$ - $C_3$  rises. The charge current is limited by  $R_5$ , while  $D_3$ - $D_4$  form a voltage doubler, so that several hundred volts are available across the contact of  $Re_1$ . LED  $D_5$  lights to indicate that the flash capacitors are fully charged, and that  $S_1$  may be released. When the fire button,  $S_2$ , is pressed,  $Re_1$  is energized, and a short pulse of 50-100 A is passed through the loudspeaker's voice coil. Make sure that this can handle the current surge, on penalty of once and for all destroying the cone suspension.



87518

The current consumption of the starting-pistol simulator is about 3 A immediately after pressing  $S_1$ , and gradually falls to 0.5-0.8 A when the reservoir capacitors contain their nominal charge. The loudness of the bang can be increased by raising the supply voltage to a

maximum of 12 V, provided the loudspeaker can handle a peak power of more than 1,000 W. It is recommended to test the circuit at a supply voltage of 3 V. Finally, bear in mind that the generated high voltage is extremely dangerous, and requires due attention to be paid

to proper insulation of all components in the high voltage section.

B

By R Shankar

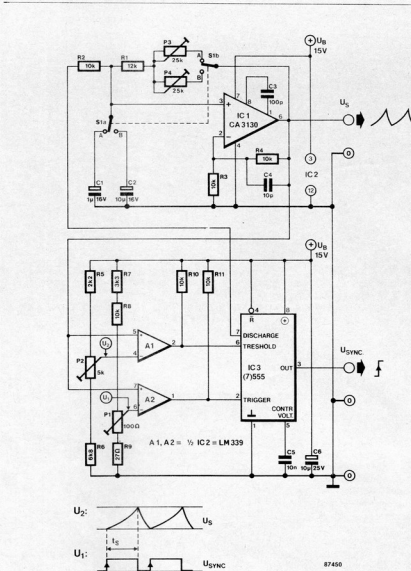
This circuit outputs a logarithmic signal for driving the VCO input on the Elektor Electronics Function Generator<sup>(1)</sup>, but can be used for other generators as well. Usually, the exponential function is derived from the (temperature-sensitive) B-E junction in a transistor, but this design uses a simple R-C network and an opamp to generate the logarithmic sweep.

With reference to the circuit diagram,  $U_s$  is applied to the generator's VCO input, while  $U_{sync}$  is used for triggering an oscilloscope on the positive signal edge. Contrary to the Elektor Electronics Sweep Generator in<sup>(2)</sup>, the timebase of the scope is used for the horizontal deflection, so that the horizontal (frequency) axis has a logarithmic scale. The sweep range is 1:100 ( $U_{VCO}=0.1-10$  V). Opamp IC<sub>2</sub> is dimensioned for a gain of 2 ( $R_3=R_4$ ) and generates an sweep voltage,  $U_s$ , with the aid of network  $P_2/P_1R_1C_1/C_2$ :

$$U_s = U_1 \exp(t/R_1C_1) \text{ when} \\ U_1 \leq U_s \leq U_2$$

When  $U_s$  reaches level  $U_2$  the bistable in IC<sub>1</sub> is reset. Capacitor  $C_1$  (or  $C_2$ ) is then discharged via  $R_2$  and the discharge input on the 555 (or 7555) until  $U_s = U_1$ , causing IC<sub>1</sub> to be set and the next sweep period to commence. The output of the monostable supplies the trigger signal for the oscilloscope.

To adjust the circuit, set the function generator to 100 Hz; external frequency. Connect the VCO input to the wiper of  $P_1$  (do not forget the ground connection), and adjust this preset for an output frequency of 100 Hz. Next, connect the VCO input to the wiper of  $P_2$ , and adjust this preset for an output frequency of 10 kHz. Proceed with connecting the oscilloscope, set to 10 ms/div., external trigger. The sweep voltage



is applied to the Y input, and the vertical sensitivity is adjusted until the maximum excursion of  $U_s$  reaches the top of the display. Set  $S_1$  to position A (sweep 0.1 s), and adjust  $P_1$  until the peak of the exponential voltage is displayed in the top right-hand corner. This is repeated with  $S_1$  set to position B (sweep 1 s), and the scope set

to 100 mV/div. (adjust  $P_2$ ). This completes the adjustment procedure, and  $U_s$  can be connected to the VCO input. The current consumption of the circuit is less than 25 mA or 15 mA with a 555 or a 7555 fitted, respectively.

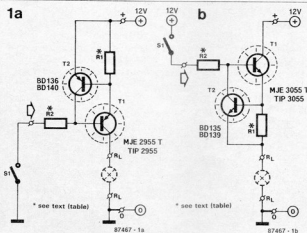
Th

## References:

- (1) *Function generator*. Elektor Electronics, December 1984.
- (2) *Audio sweep generator*. Elektor Electronics, November 1985.

87450

Motorist are generally well aware that car fuses do not blow just like that. None the less, when something appears to be amiss in the electrical circuit, a new fuse is nearly always fitted prior to investigating the possible cause for the malfunction, which then, of course, costs two fuses. The circuits shown here are short circuit proof power switches, or electronic fuses with switch control dimensioned for relatively heavy (lamp) loads in a car. Both circuits are composed of a power switch,  $T_1$ , and a current limiter,  $T_2$ . The circuit is fully short-circuit and overload resistant, provided  $T_1$  is adequately cooled, and the whole unit is constructed in a sturdy enclosure. The circuit in Fig. 1a has the lower voltage drop of the two, while that in Fig. 1b is used when a TO-218 style Type MJE2955T or TIP2955 is not obtainable. It is interesting to note that the plastic TO-218 package is mechanically interchangeable with the well-known TO-3 outline, and enables ready mounting of the



## Part list

Resistors ( $\pm 5\%$ ): $R_1, R_2$  = see text

Semiconductors:

 $T_1$  = MJE2955T or TIP2955 (Fig. 1a) $T_1$  = MJE3055T or TIP3055 (Fig. 1b) $T_2$  = BD136 or BD140 (Fig. 1a) $T_2$  = BD135 or BD139 (Fig. 1b)

Miscellaneous:

 $S_1$  = see text

PCB Type 87467 (not available through the Readers Services).

transistor onto a flat surface using an insulating washer—see Fig. 2. The use of a die-cast enclosure and TO-3 style transistors is illustrated in Fig. 3. This unit houses two power switches, one of which has its contacts at the rear side. Pay great attention to the correct electrical insulation between the transistors and the enclosure, and, if required, that

between the enclosure and the car body. Switch  $S_1$  is the existing control for the relevant lamp in or on the vehicle. Note the difference in respect of the connection of  $S_1$  in Fig. 1a and 1b. Table 1 shows how  $R_1$  and  $R_2$  are dimensioned in accordance with the current requirement of

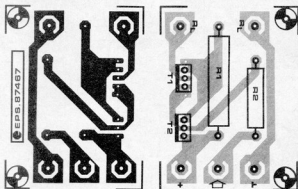
the load, and also gives a suggested area of the cooling surface.

Finally, when the printed circuit board is used,  $T_1$  should be a TIP2955 or a MJE2955T, not a MJE2955, since this has its outer terminals (B-E) reversed.

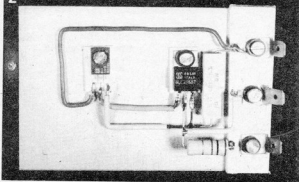
$F_e$

Table 1

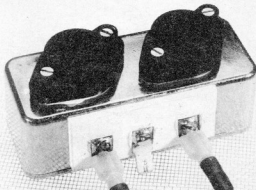
Application	$R_1$ [W]	$I$ [A]	$R_1$ [ $\Omega$ ]	$R_2$ [ $\Omega$ ]	Cooling $T_1$ - $T_2$
Dashboard lighting	1	0.08	5.6	3300	not required
Courtesy light	2	0.17	2.7	1500	not required
Rear light or parking light	5	0.42	1.2	680	25 cm <sup>2</sup>
Brake light	18	1.5	0.33 (5 W)	180 (1 W)	225 cm <sup>2</sup>
Fog light or trafficator	21	1.75	0.27 (5 W)	150 (1 W)	225 cm <sup>2</sup>



2



3



The Sinclair Quantum Leap (QL) computer is eminently suitable for a low-cost introduction into working with Motorola's 68000 true 16-bit microprocessor. Many computer enthusiasts did not fail to note the spectacular price cuts for the QL when its production was discontinued. An excellent support program, TOOLKIT II, became available and is still considered indis-

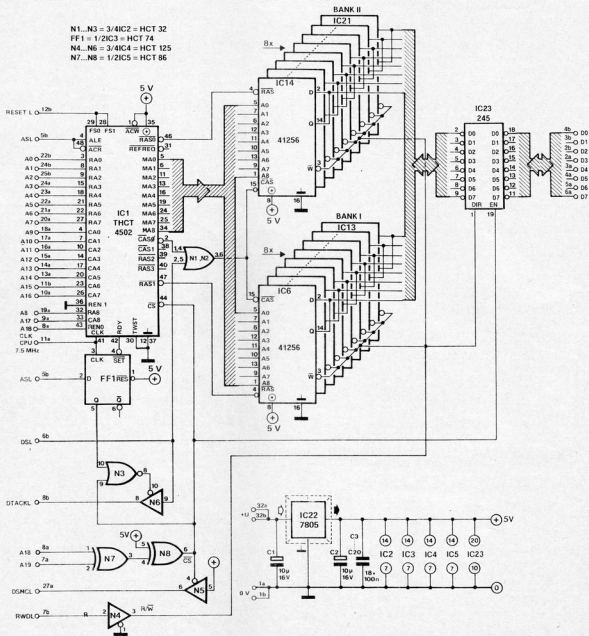
pensable by many for getting to grips with the QL. The present 512 Kbyte RAM extension should be very welcome for running a RAM disk, and/or programs such as ICE and QIMP.

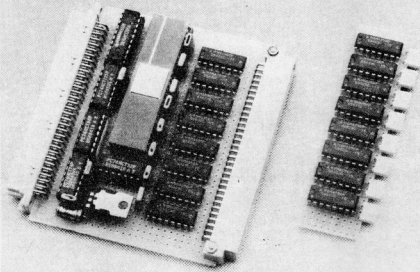
The circuit is based around the Type THCT4502 RAM controller from Texas Instruments. This dedicated controller takes care of all the DRAM controlling.

including the refresh timing, and the address line multiplexing. The address decoder is made with a single XOR gate,  $N_7$ . The DSMLC line is made high within 30 ns with the aid of three-state buffer  $N_8$ . Bistable FF<sub>1</sub> delays the ASL signal somewhat, so that DTACL is only activated when the RDY output of IC<sub>1</sub> is stable. The databus is buffered by bidirectional octal

transceiver IC<sub>23</sub>

The extension memory is divided in two banks of 256 Kbyte. Note that CAS, unlike RAS, is common to both banks. It is possible on the QL to omit the second bank without altering the address decoding. This is thanks to QDOS, which searches for correctly operating, continuous, and unique, i.e. non-mirrored, memory. It is





interesting to note that machine code in the extension memory runs at almost double the normal speed.

The RAM chips used should have an access time of 150 ns or less. Current consumption of the extension is low at 50 mA or 150 mA in the non-active and active mode respectively. Non-used inputs on gates should be tied to ground.

Finally, note that the Type THCT4502 controller may not be available everywhere yet. *W*

Distributor for TI Semiconductors in the UK is DC Distribution

• Freepost • Hitchin Road  
• Arlesly • Bedfordshire SG15  
6BR. Telephone: (0462) 834444  
or (0454) 273333.

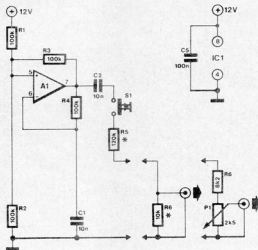
## 84

# SYNCHRONIZED SLIDE CHANGER

Sound and vision can be synchronized fairly easily for making slide presentations: the left and right channel of a cassette or tape recorder are used for separate recording and playing back of the music and accompanying speech, and the slide change control signal. The circuit around  $A_1$  is a square wave generator that produces the 1 kHz slide change signal for recording on one track of the tape.  $S_1$  is pressed when the next slide is to appear. Voltage divider  $R_3$ - $R_4$  ensures that the recording amplifier is not over-driven. If necessary,  $R_4$  can be replaced by a 8K2 resistor and a 2K5 potentiometer as shown to enable adjusting the output amplitude.

The circuit around  $A_2$  is the playback amplifier for driving the slide change relay. The quiescent current of the slide changer is about 15 mA.

Some projectors have a slide feeder that can be moved in reverse with the aid of two short control pulses, or one long pulse. This is of course also possible with the present circuit.



A 1, A 2 = IC 1 = 3240  
Re 1 = 12 V, max. 80 mA

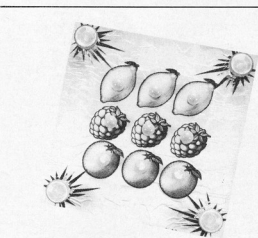
By F Pipitone

This is one of the very few "one-armed bandits" to which the maxim *the sole way to win is not to gamble* is not applicable. In other words, this circuit does not have a slot for inserting coins; every play is free.

Actuation and release of the "PLAY" button,  $S_1$ , causes the circuit to become operative. Series regulator  $T_1$  is driven into saturation by  $T_2$ , which is controlled by  $N_7$ . The outputs of  $N_2$ ,  $N_{11}$ , and  $N_{15}$  go high in succession, and disable counters IC<sub>3</sub>, IC<sub>4</sub> and IC<sub>5</sub>, which are all clocked by oscillator  $N_{12}$ - $N_9$ , and reset by the pulse at their  $Q_3$  output. The 3 LEDs driven by each of the counters are, therefore, illuminated cycli-

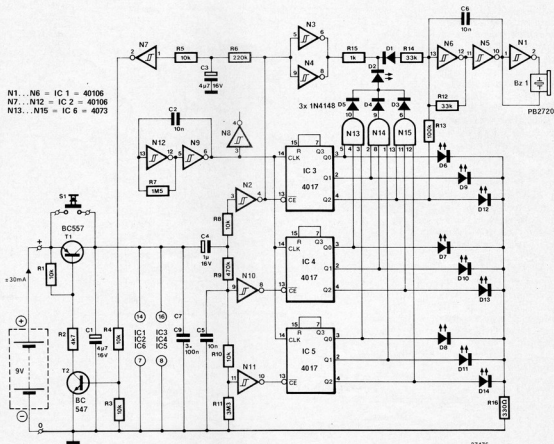
cally. When a counter is disabled by the high level at its CE input, one of the LEDs in the 3 groups remains illuminated. The output state of the counters is not predictable because of the inconstant delay between the disable instants. NAND gates  $N_{13}$ - $N_{15}$  detect the winning combinations, i.e., LED  $D_2$  is illuminated, and  $Bz_1$  is sounded, when 3 identical counter outputs are activated. Note that diodes  $D_3$ - $D_5$  form a 3-input OR gate, and that the buzzer also produces sound when the LEDs are flashing, since the pulses at output  $Q_2$  of IC<sub>3</sub> enable the oscillator intermittently.

The play is ended when the voltage across  $C_3$  is high enough for gate  $N_7$  to change



state.  $T_2$  is turned off, and  $T_1$  no longer powers the circuit. An on/off switch is not required for

the fruit machine, thanks to its very low current consumption in the de-activated state. R





## Parts list

### Resistors ( $\pm 5\%$ ):

R1; R3; R4; R5; R8; R10 = 10K  
R2 = 4K7  
R6 = 220K  
R7 = 1M5  
R9 = 470K  
R11 = 3M3  
R12; R14 = 33K  
R13 = 100K  
R15 = 1K0  
R16 = 330R

### Capacitors:

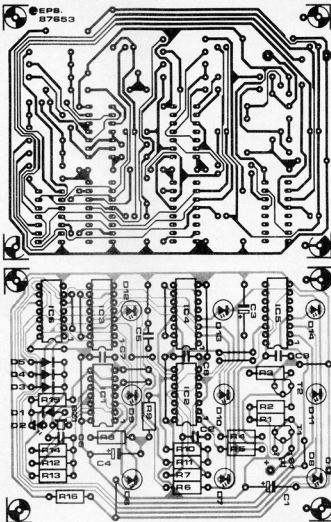
C1; C3 = 4 $\mu$ 7; 16 V; axial  
C2; C5; C6 = 10n  
C4 = 1 $\mu$ ; 16 V; axial  
C7; C8; C9 = 100n

### Semiconductors:

D1; D3; D4; D5 = 1N4148  
D2; D6; D7; D8 = LED (red)  
D9; D10; D11 = LED (yellow)  
D12; D13; D14 = LED (green)  
IC1; IC2 = 40106  
IC3; IC4; IC5 = 4017  
IC6 = 4073  
T1 = BC557  
T2 = BC547

### Miscellaneous:

S1 = momentary action push button.  
Bz = PB2720 buzzer (Cirkut stock no. 43-27201).  
PCB Type 87476 (available through the Readers services).



# 86

## WEATHER SATELLITE INTERFACE

An increasing number of electronics enthusiasts is becoming interested in weather satellite reception. Most non-geostationary weather satellites, like those in the NOAA series, operate in the 138 MHz carrier. For optimum reception, the detector should feature a relatively high carrier suppression. It is assumed here that a picture signal is available on a cassette tape. Opamp A<sub>1</sub> has an amplification of 48, while A<sub>2</sub>-A<sub>3</sub> form a precision two-phase rectifier. The 2,400 Hz ripple arising from the slightly different specification of the opamps amounts

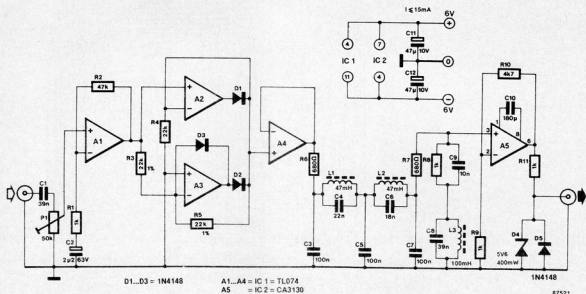
to no more than 0.2%. For commonly used A-D converters, this corresponds to an error smaller than 1/2(LSB).

The main ripple signal is 4,800 Hz. This is readily removed by a double  $\pi$  filter set up around L<sub>1</sub> and L<sub>2</sub>. At 2,500 Hz, the attenuation is about 3 dB, at 4,500 Hz about 45 dB. The parallel R-C and L-C networks at the + input of A<sub>3</sub> compensate for the ohmic resistance of the inductors in the  $\pi$  filter. L<sub>1</sub>, L<sub>2</sub> and L<sub>3</sub> are preferably ferrite-encapsulated chokes from the Toko 10RB series, available from Cirkut PLC (L<sub>1</sub> & L<sub>2</sub>: 181LY-473. L<sub>3</sub>:

181LY-104). The interface is suitable for processing carrier frequencies up to 4,800 Hz, so that it is possible to play the tape at double speed for reading into the computer (provided, of course, the program can handle this). Components R<sub>11</sub>, D<sub>4</sub> and D<sub>5</sub> protect the A-D converter against voltages higher than 5 and lower than 0 volt. The use of the Type CA3130 BiMOS opamp ensures an output voltage swing of 5 V when a  $\pm 6$  V supply is used. The maximum supply level and current consumption are  $\pm 9$  V and 15 mA respectively. The

input signal amplitude should be greater than 68 mV<sub>rms</sub> for a 5 V<sub>pp</sub> output.

B



87521

# 87

## INSTRUMENTATION AMPLIFIER

This instrumentation amplifier was originally designed for the serial digitizer described in <sup>(1)</sup>, but should be suitable for many other applications also. The amplifier makes it possible to use a relatively long, interference-free, connection between the transducer or sensor and the digitizer input.

The theoretical basis for the circuit is summarized in the accompanying Table. It is seen that the common mode rejection of the amplifier serves to suppress interference. In practice, however, the low drive margins of the inputs and outputs of the opamps impose some limitations. Both suggested types have PNP input transistors capable of handling input voltages between 0 and  $U_b - 1.5$  V. The output of the OP-220 can deliver voltages between 0 and  $U_b - 1$  V, that of the LM358 between 0 and  $U_b - 1.5$  V.

The current consumption of the opamps is low at about 150  $\mu$ A for the OP-220, and 1 mA for the LM358, while the slew rate is about 0.04 V/ $\mu$ s and 0.4 V/ $\mu$ s respectively. For optimum accuracy it is recommended to use high stability (1%) resistors in positions R<sub>1</sub>-R<sub>5</sub> inclusive.

### Reference:

<sup>(1)</sup> *Universal peripheral equipment (2): Serial Digitizer*. Elektor Electronics, September 1986 p. 23 ff.

### Micropower instrumentation amplifier

Consider an input  $U_{CM} = \frac{1}{2}U_d$  at the  $-$  input of the circuit, and  $U_{CM} + \frac{1}{2}U_d$  at the  $+$  input. This corresponds to a common mode input  $U_{CM}$ , and a differential input  $U_d$ . The currents at the inverting input of each opamp can be summed to form two equations:

$$(U_b - U_{CM} + \frac{1}{2}U_d) \cdot (1/R_1) + (U_d/R_0) + (U_b + \frac{1}{2}U_d) \cdot (1/R_3) = (U_{CM} - \frac{1}{2}U_d) \cdot (1/R_2) \quad (1)$$

$$(U_b - U_{CM} - \frac{1}{2}U_d) \cdot (1/R_4) + U_b \cdot \frac{1}{2}U_d \cdot (1/R_5) = U_d/R_0 \quad (2)$$

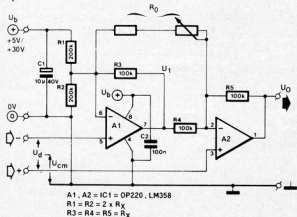
When  $R_1 = R_2 = 2R_3 = 2R_4 = 2R_5 = 2R_x$ , (1) and (2) can be combined to

$$U_b = 2(1 + R_x/R_0)U_d + \frac{1}{2}U_b$$

which shows that the common mode input ( $U_{CM}$ ) has been rejected. The differential gain,  $A_x$ , of the circuit is therefore

$$A_x = 2 + (2R_x/R_0)$$

and is adjustable between 0 and 1,000 by varying  $R_0$ .



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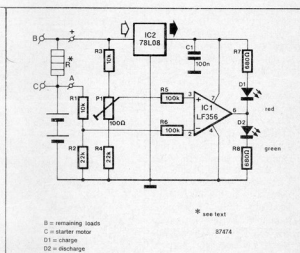
PMI Application

By R Baltissen

Many of today's cars and motor cycles are equipped with a meter for monitoring the battery voltage. However, this meter does not provide information on the battery condition, or whether it is being charged at all. When the voltmeter reading is too low, the battery is generally in such a poor state as to necessitate switching off heavy loads to save power for use of the starter engine later. Especially on motorcycles, the battery capacity is relatively low, which justifies the need for a reliable monitoring system. A standard 30 A ammeter offers too low resolution, and is rather awkward to fit permanently. In this charge/discharge indicator, the measured current is converted into a potential differ-

ence by  $R_7$ , which is either two 100 5 W resistors, a fuse, or a few turns of copper wire. The direction of the current through  $R_7$  is detected by comparator IC1, which then indicates whether the battery is being charged or discharged by lighting the relevant LED. The 100R preset enables shifting the indication threshold somewhat. Input terminal + on the indicator unit is best connected to a point behind (that is, electrically behind) the contact switch, although it is also possible to fit the circuit with a separate on/off switch. Finally, the circuit is only suitable for use in or on vehicles having a 12 V battery.

R



Integrated operational amplifiers are not always suitable for applications where a high signal level ( $U_o \leq 10 V_{rms}$ ) is required for driving a relatively low impedance ( $Z = 50-600 \Omega$ ). The amplifier described here is eminently suitable as a high dynamic range line driver or power buffer in public address systems and AF distribution amplifiers.

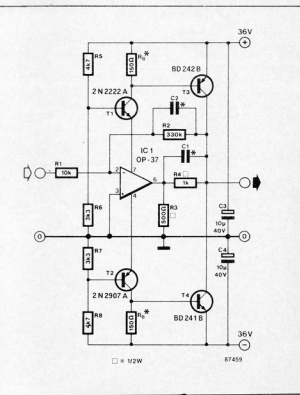
The input amplifier of the line driver is formed by a low noise opamp Type OP-37 from PMI. This ensures the following technical specification of the line driver:  $U_o = 70 V_{pp}$  max.;  $I_o = 400 mA_{pp}$  max.;  $D_{tot} = 0.01\%$  at  $U_o = 10 V_{rms}$ ,  $Z_L = 50 \Omega$  and  $S/N \geq 90$  dB.

Regulators  $T_1, T_2$  bring the supply voltage for the OP-37 down to  $\pm 15$  V. The complementary power output stage is formed by  $T_3, T_4$ . The amplifier has a standard negative feedback circuit  $R_1, R_2$ , which results in a voltage gain  $A_v = -(R_2/R_1)$ . A local feedback  $R_3, R_4$  has been included to keep the output voltage of the

opamp within safe limits, while capacitors  $C_1, C_2$  serve to improve the stability. It should be noted that the value of  $C_1$  and  $C_2$  depends on the construction of the line driver: typical values are 680 pF for  $C_1$  and 22 pF for  $C_2$ . In a prototype of the circuit, neither capacitor was required for the frequency response to remain flat ( $\pm 1$  dB) up to 100 kHz.

Resistors  $R_5$  should drop just enough voltage for  $T_3$  and  $T_4$  to start conducting (class A-B operation). The quiescent current of IC1 is about 3 mA, so that 150  $\Omega$  can be taken as a suitable starting value for  $R_5$ . The quiescent current in the power output stage should be between 20 and 50 mA. Higher values of  $R_5$  cause the quiescent current, and hence the power dissipation, to increase, resulting in less distortion. The power output stage is not protected against thermal overloading, so that due care should be taken in adjusting the quiescent current.

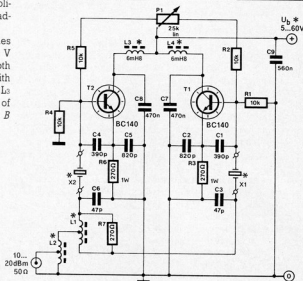
Sv



This test oscillator is useful to ensure optimum operation of RF amplifier stages designed to work on the short-wave bands. Based on two crystal oscillators, it provides considerable output power (10 to 100 mW) to enable measuring intermodulation characteristics of high level and RF power stages. The quartz crystals used here not only serve as the frequency determining elements (2...20 MHz), but also as output filters to prevent one generated signal being lost in the other oscillator. With this in mind, tapped inductors  $L_1$  and  $L_2$  ensure freedom of mutual interference when the oscillator is used for frequencies higher than 10 MHz. Both inductors are wound as 12 turns of enamelled copper wire with a centre tap, on either a small balun or a suitably rated core with an air

gap. Outputs of equal amplitude can be obtained by adjusting  $P_1$ .

The test oscillator consumes about 250 mA from a 60 V supply. This means that both transistors should be fitted with a heat-sink, and that chokes  $L_3$  and  $L_4$  should be capable of carrying about 150 mA. *B*



\* See text

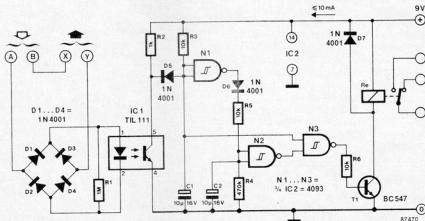
87478-A

In this circuit, a relay is energized when a call signal is received, or when the receiver is lifted. The relay remains energized for a short period after ringing off and after the call signal has ended. An optocoupler is used here in view of the direct connection to the telephone line, and the rela-

tively high bell voltage on it. Current is passed through the LED in IC<sub>1</sub> via rectifier  $D_1$ ... $D_4$ , so that the phototransistor conducts.  $C_1$  is discharged via  $D_5$ ,  $N_1$  changes state, and  $T_1$  energizes the relay. Also,  $C_2$  is charged via  $D_6$ , and so ensures that the lamp remains illuminated for a few seconds after

the receiver has been put on the rest, or after the bell signal has ended. The current consumption of the circuit in the stand-by mode is less than 10 mA. The coil voltage of the relay should be equal to the supply voltage used. *Sr*

**Note:** connection of this circuit to the British Telecom telephone network is not permitted.



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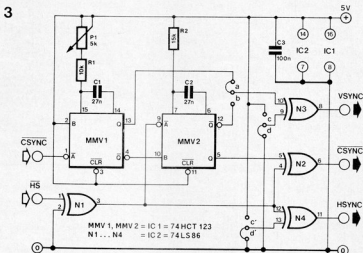
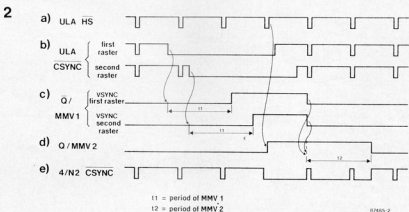
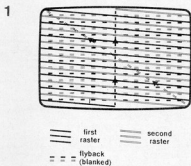
Owners of the Acorn Electron home computer may well object to its interlaced, and therefore slightly instable, picture. There is a trace of display flicker in non-moving areas on the screen, and this is mainly due to the internal video processing circuitry operating on the basis of interlacing, a technique used in conventional TV transmission for smoothing the appearance of moving picture areas. Arguably, interlacing is not very useful in computers, since these work with text in most applications. Special displays with a relatively long afterglow time are no remedy for this awkward problem, and that is why the present circuit was designed. It effectively switches off the interlace function, and so ensures a restful display, albeit that the individual lines that make up the characters become slightly more prominent.

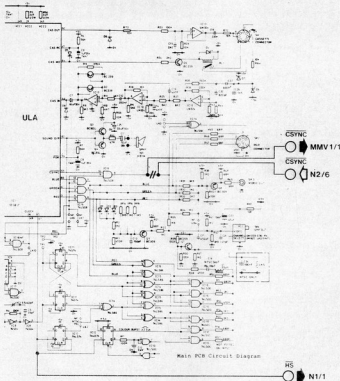
Figure 1 shows that a TV picture is composed of 625 lines divided between 2 rasters of 312.5 lines each. In an interlaced picture, these rasters are vertically shifted by one line. This is done by starting the second raster  $x$  and a half time later than the first raster. Interlacing can thus be rendered ineffective by starting the second raster half a line period earlier (i.e., after 312 lines rather than 312.5). To retain the normal number of lines (625), the second raster is arranged to comprise 313 lines.

The ULA chip (Uncommitted Logic Array) in the Electron computer provides a horizontal and a composite synchronization signal, which are shown in Figs. 2a (HS) and 2b (CSYNC) respectively. With reference to Fig. 2c, and the circuit diagram in Fig. 3, MMV1 forms a new vertical synchronization pulse, VS, with the aid of the CSYNC signal. The period of pulse VS is different for the first and second raster, so that MMV2 is needed to make VSYNC equally long in both. MMV2 is triggered on the first line pulse (HS) that occurs when VS is active, and is retriggered when VS goes low—see Fig. 2d. The

length of the VSYNC pulse so made is about 160  $\mu$ s, or about 2.5 times the line time (64  $\mu$ s). The HS and the new VS signal are combined in XOR gate N2 for driving the video modulator. Gate N1 serves to buffer the HS output of the ULA.

The final results obtained with the circuit depend mainly on the type of TV set or display used, and may not be optimum when the TV is driven via its RF input. On an older type monochrome set, the central area of





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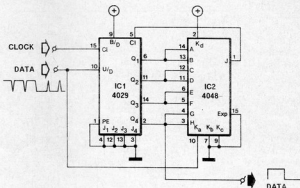
the picture was stable, but the upper and lower areas gave a less favourable look. Good results were obtained, however, from the use of Type TX chassis, which are currently the basis of TV sets sold under many different names and licenses. Even better performance can be expected from a video monitor, whose (TTL compatible) H and V synchronization inputs can be driven by  $N_4$  and  $N_3$  respectively. The polarity of the sync signals can be selected with the aid of wire jumpers. Connections c and c' result in VSYNC and HSYNC. The choice between jumper a or b depends on the type of display used. Preset  $P_1$  is adjusted until the picture appears vertically synchronized; the adjustment is fairly critical when jumper a is used. The final results obtained with the circuit can be judged from looking at a few characters in the upper and lower area of the screen. The modest current consumption of the circuit, 10 mA, makes it possible to power it direct from the Electron computer. **TW**

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## DEGLITCHER

Extremely short, unwanted, pulses with a period in the nanosecond range are often referred to as *glitches*, and occur in most, if not all, digital circuits. Whilst the circuit in question can be designed and built with due attention paid to effective suppression of glitches, it is not always possible to foresee the effects of external noise on, for instance, a clock signal. The filter presented here effectively rules out the presence of glitches in a serial data link.

Assuming that counter IC<sub>1</sub> is at state nought, and that the data input is logic high, IC<sub>2</sub> is configured as an AND gate. Output Q<sub>4</sub> of IC<sub>1</sub>, and hence the output of the deglitcher, goes high after 8 clock pulses. A short negative pulse at the data input merely results in a few more clock pulses being required before Q<sub>4</sub> is activated. After another 8 clock pulses, the



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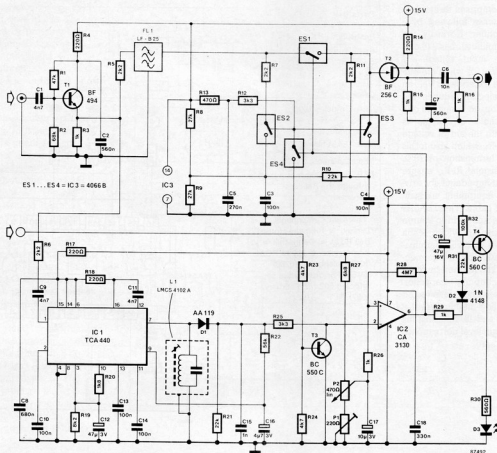
counter state is 15. This causes the C<sub>I</sub> (CARRY IN) input of IC<sub>1</sub> to be driven high, so that the clock signal remains blocked as long as the data input is logic high. When it goes low, IC<sub>2</sub> is configured as a NOR gate, enabling the clock transitions to be counted down in IC<sub>1</sub>. Out-

put Q<sub>4</sub> goes low again after 8 clock pulses, and the counter is blocked after another 8 pulses. Therefore, the filtered output data is delayed by 8 clock periods, but this is insignificant in the proposed application. The data frequency,  $f_{D1}$ , depends on the clock frequency,

$$f_{D1} = f_{CLK} / 16$$

$$f_{D1} = f_{CLK} / 16$$

The maximum usable clock frequency is about 8 MHz. The current consumption of this circuit is less than 1 mA **B**



A noise blanker is indispensable for improving the reception of very weak signals on the SW bands. In most communication receivers, the selectivity of intermediate frequency (IF) filters causes interfering pulses to be widened, blotting out the wanted signal. It is useful, therefore, to suppress interference before this can wreak havoc in the IF sections of the receiver.

The 455 kHz IF signal is first buffered in T<sub>2</sub>, and then processed separately in two circuits.

The lower section of the circuit is a TCA440 based receiver for the interfering pulses. The

TCA440 is in itself a virtually complete receiver, since it comprises an RF amplifier, a mixer, and an IF amplifier. All stages in the latter are used since pin 4 is grounded here. The pulse receiver has its own AGC (automatic gain control) to ensure effective suppression of relatively weak interference also. Preset P<sub>1</sub> and potentiometer P<sub>2</sub> enable precise adjustment of the noise blanker for various levels of interference. The circuit can be controlled digitally via R<sub>23</sub>; a logic high level renders the noise blanker ineffective. The interfering pulses are made logic

compatible with the aid of opamp IC<sub>2</sub>. LED D<sub>3</sub> lights when noise is detected.

In the upper section of the circuit, the IF signal is first delayed in FL<sub>1</sub> to compensate for the processing time in the pulse receiver. ES<sub>1</sub> is opened when a sufficiently strong interfering pulse is recognized, so that the IF signal is no longer applied to output buffer T<sub>2</sub>. Also, the gate of this FET is then grounded for RF signals via ES<sub>3</sub>-C<sub>4</sub>, while ES<sub>2</sub> is closed to maintain correct termination of FL<sub>1</sub>.

Properly constructed, this circuit achieves noise suppression of the order of 85 dB. Alterations

to suit operation at an IF other than 455 kHz merely involve L<sub>1</sub> and FL<sub>1</sub>, although due account should be taken of the parasitic capacitance of the electronic switches at relatively high frequencies.

B

The Type TEA5114 from Thomson-CSF comprises three electronic switches followed by a buffer/amplifier. Normally the voltage amplification is 2 (6 dB). When the input voltage exceeds  $1.2 V_{DD}$ , or when the output voltage exceeds  $1.5 V_{DD}$ , an internal selector reduces the amplification to unity (0 dB). The threshold of  $1.2 V_{DD}$  is created with the aid of voltage divider  $R_1$ - $R_3$ , which also forms the input termination of  $75 \Omega$ . Series resistors  $R_1$ - $R_3$  ensure  $75 \Omega$  output impedance for driving video equipment via standard coax cable. The TEA5114 can be used as a video source selector also, provided each input has its own  $75 \Omega$  termination network. The non-connected inputs should then be fitted with a coupling capacitor. Channel selection is effected by controlling the logic level at pins 10, 12 and 15. Note that the logic 1 (high) level corresponds to  $+2.5 V$  here.

D

#### Parts list

Resistors ( $\pm 5\%$ ):

$R_1 \dots R_3$  incl. =  $15 \Omega$

$R_4$  =  $47 \Omega$

$R_5$  =  $27 \Omega$

Capacitors:

$C_1 \dots C_4$  incl. =  $100 n$

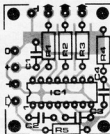
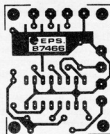
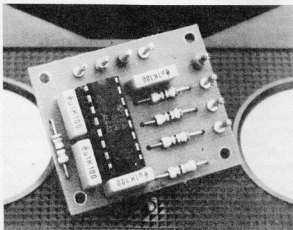
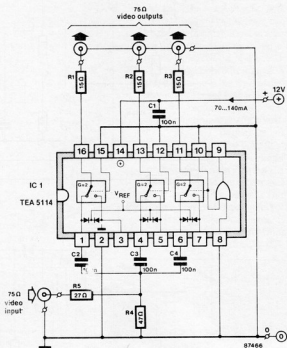
Semiconductor:

IC<sub>1</sub> = TEA5114\*

Miscellaneous:

PCB Type 87466 (not available through the Readers Services).

\* Thomson Components Limited • Ringway House Bell Road • Darneston • Basingstoke • Hants RG24 0QG. Telephone: (0256) 29155. For distributors see Infocard 502 (EE February 1987).



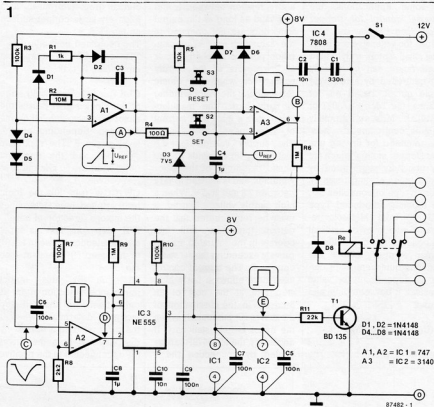


This two-key wiper delay circuit is remarkable for its simplicity and ease of use. The wiper is started by pressing the SET switch, which also serves to adjust the length of the wipe interval. The circuit is turned off by pressing the RESET button.

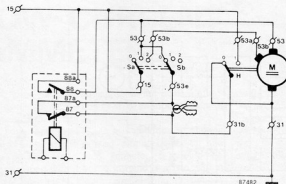
The wiper delay shown in Fig. 1 consists of three opamps and a monostable multivibrator (MMV). Opamp A<sub>1</sub> is set up as a triangular wave generator, controlled by the output of the MMV. When this is low, a slowly rising sawtooth voltage appears at the output of A<sub>1</sub>. The rise time of the sawtooth depends on R<sub>2</sub>-C<sub>3</sub>. Opamp A<sub>3</sub> compares the voltage across C<sub>4</sub> to the instantaneous sawtooth amplitude. The output of A<sub>3</sub> drops from 8 V to 0 V when the sawtooth voltage exceeds U<sub>IC4</sub>. This change in the output voltage of A<sub>3</sub> is delayed by R<sub>6</sub>-C<sub>6</sub> and passed to A<sub>2</sub>, so that the MMV is triggered somewhat later. The wipers are switched on via T<sub>1</sub> and R<sub>6</sub> when pin 3 on the 555 is delayed by R<sub>6</sub>-C<sub>6</sub> and passed to A<sub>2</sub>, so that the MMV is triggered somewhat later. The wipers are switched on via T<sub>1</sub> and R<sub>6</sub> when pin 3 on the 555 is delayed by R<sub>6</sub>-C<sub>6</sub> and passed to A<sub>2</sub>, so that the MMV is triggered somewhat later.

When the circuit is first switched on, C<sub>4</sub> is discharged, and the output of A<sub>1</sub> is slightly higher than 0 V due to V<sub>IC-E</sub> of the internal output transistor. This causes the outputs of A<sub>3</sub> and A<sub>2</sub> to remain low, so that the wiper relay remains energized initially. When RESET is pressed, C<sub>4</sub> is charged via R<sub>5</sub>, causing the output of A<sub>3</sub> to go high, and the MMV to be stopped. The delay circuit around A<sub>2</sub> is necessary to prevent C<sub>4</sub> being discharged completely after pressing the SET button.

The relay contacts should be wired such that the dashboard switch is by-passed when the relay is energized, and that the hold switch, H, for the wiper motor is opened—see Fig. 2. Due attention should be given to the correct connection of the hold switch on penalty of short-circuiting the car battery. R



2



For some applications, the *Universal control for stepper motors* (see <sup>[1]</sup>) may be considered too extensive a circuit. Many small motors with limited speed range can be equally well controlled by a relatively simple circuit, based on, for instance, the Type SAA1027 or TEA1012 <sup>[2]</sup>. Most commercially available controllers are, however, intended for driving unipolar stepper motors, which are now gradually superseded by bipolar types of similar size. In different type of controller. The recently introduced Type MC3479P from Motorola requires a minimum of external components for controlling a bipolar stepper motor. The maximum quiescent stator current,  $I_s$ , depends on the value of resistor R between pin 6 and ground:

$$I_s = (U_b - 0.7) / 0.86R \text{ [mA]}$$

where R is given in k $\Omega$ . The

above relation between  $I_s$  and R is valid as long as the output transistors are not operated in the saturated area. The saturation point is reached sooner at low levels of the supply voltage, or when the ohmic resistance of the stator winding is fairly high. The manufacturers state a maximum current of 350 mA per stator.

The supply voltage for the motor (pin 16) depends on the ohmic resistance of the stator windings, and is allowed to vary between 7.2 and 16.5 V. When a high supply voltage is used, it must be remembered that the output transistors will not operate in the saturated area to prevent exceeding the set stator current,  $I_s$ . The current control used here allows a fairly high step rate at the cost of an increase in the dissipation of the driver IC, particularly when the motor is held stationary. If necessary, the MC3479P can be cooled by connecting the 4

central ground terminals to a relatively large copper surface on the PCB.

The integrated controller has 4 TTL and CMOS compatible inputs (see Fig. 1):

**CLK** (pin 7): every rising edge of the clock signal causes the motor to revolve one full or one half step, depending on the level at pin 9. The maximum step rate and the minimum pulse width are 50 kHz and 10  $\mu$ s respectively.

**CW/CCW** (pin 10): the logic level applied here determines the motor's direction of travel.

**F/H step** (pin 9): this input allows selection between full (0) or half step (1) operation—see Fig. 3.

**OI** (pin 8): this output impedance selection input is only effective in the half step mode. It determines whether the stator winding is effectively disconnected from the driver (0), or connected to the positive

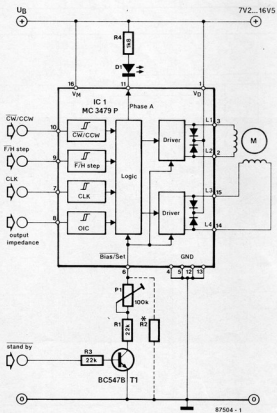
supply at both ends (1). The latter option improves the damping of the motor in the half step mode, and will prove useful at relatively low step rates.

Pin 11 of the driver IC is an open-collector output with a current capacity of 8 mA, activated during period A in Fig. 3. A LED connected to this output will flash rhythmically when the motor is running.

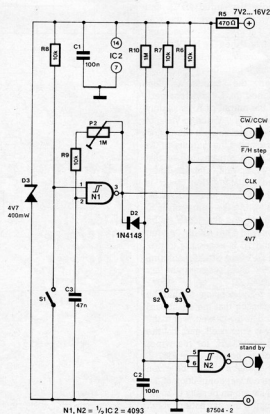
Transistor T<sub>1</sub> was added to obtain a reset function. No stator current flows, and the logic circuitry in the driver is reset, when the stand by input is driven low. When a logic 1 is applied, the motor is energized starting from state A. The addition of R<sub>2</sub> makes it possible to switch the driver to the power-down state, rather than the reset state. The stator current is reduced to the value set with R<sub>2</sub>, as shown in the above formula.

The motor driver is probably best controlled by a computer

1



2



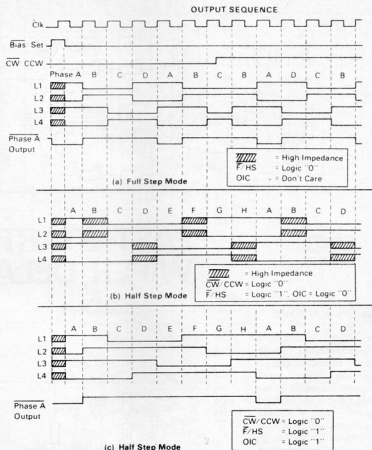
output port. The circuit in Fig. 2 is intended for stand-alone applications. It is composed of a supply,  $R_5$ - $D_3$ , an oscillator,  $N_1$ - $C_3$ - $R_6$ - $P_2$ , and a re-triggerable monostable multivibrator,  $N_2$ - $C_2$ - $R_{10}$ - $D_2$ . When  $S_1$  is opened, the oscillator is enabled, and the motor will start running. The clock frequency, i.e., the step rate, is adjustable with  $P_2$ . The monostable will remain set via  $D_2$ , and  $T_1$  will conduct, as long as clock pulses are applied to the motor driver. The amount of ever reversing stator current is limited by the stator inductance, but can be still be increased with the aid of  $P_1$ . When the motor stops,  $T_1$  is turned off, and the stationary stator current is reduced to the value set with  $R_2$ . The above arrangement keeps the dissipation of the motor and the driver within reasonable limits.

The current consumption of the complete circuit is practically that of the motor alone (700 mA max.). The motor driver IC consumes about 70 mA. *TW*

#### References:

- [1] *Universal control for stepper motors*. Elektor Electronics, January 1987.
- [2] *Stepper motor control*. Elektor Electronics, July/August 1986.

3



87504-3

98

## LOW CURRENT AMMETER

This 7-range ammeter measures currents between a few pA to 100  $\mu$ A without using precision resistors with very high values. The circuit is set up around a current mirror  $T_{1A}$ - $T_{1B}$ . The input current is mirrored in this transistor pair, and the current through  $T_{1B}$  is greater than the input current by a factor set with  $S_1$ . Meter  $M_1$  is a 100  $\mu$ A fsd type for displaying the measured value. The effective series voltage drop at the input terminals of the instrument is only 500  $\mu$ V because the voltage across the inputs of  $A_1$  is forced to virtually nothing. The accuracy of the ammeter depends mainly on the compo-

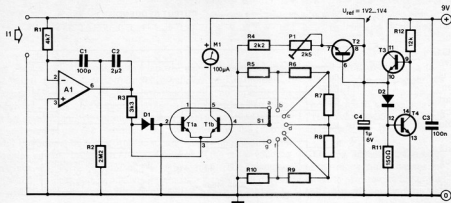
nents used. Depending on the required precision, certain components may be replaced by types with a better specification. The Type LF411 opamp used in the  $A_1$  position, for example, can be replaced with the Type OP-41 to achieve a tenfold reduction in the input bias current, and hence an improvement in the final accuracy of the instrument. Transistor pair  $T_{1A}$ - $T_{1B}$  may be replaced by a Type MAT-02, and the voltage reference set up with  $T_2$ - $T_3$  by a Type LM313. These high-quality parts should ensure an accuracy of 1% over most of the range. The meter is calibrated in the 1  $\mu$ A range. Preset  $P_1$  is

adjusted for full scale deflection of  $M_1$  at an input current of 1  $\mu$ A.

When it is intended to make a printed circuit board for the pico ammeter, it should be borne in mind that two 2.5 cm long, parallel running, copper tracks spaced 1.25 mm and etched on a high quality epoxy/glass carrier represent a leakage resistance of about 100 G $\Omega$ . This corresponds to a leakage current of 150 pA at a voltage difference of 15 V. Evidently, the PCB for the present ammeter should be thoroughly cleaned to rule out leakage current through residual moisture or resin. Also note that the

insulation of standard test leads is likely to make reliable measuring of currents smaller than 1 pA impossible. The only way to overcome this difficulty is to use dry air or PTFE (Teflon). *Sv*

Source: *PMI Linear and Conversion Applications Handbook*.



T1...T4 = IC1 = CA3046  
A1 = IC2 = LF411, OP41  
R5...R10 = 511Ω, 1%  
D1...D2 = 1N4148

S1	I1
a	100 pA
b	1 nA
c	10 nA
d	100 nA
e	1 μA
f	10 μA
g	100 μA

87507

# 99

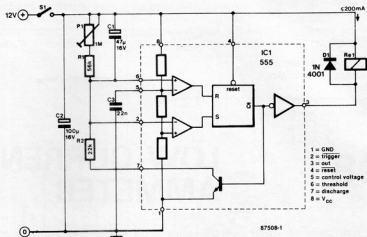
## FAST STARTING WIPER DELAY

From an idea by M. Schultz.

A wiper delay is essentially a bistable multivibrator whose off-time is adjustable with a potentiometer. Many wiper delay circuits are based on the Type 555 timer in its standard application circuit, which has the disadvantage of introducing a delay of about 1.6 times the set interval before the first wiper action takes place. This is especially annoying when an interval of, say, ten or more seconds has been set. This circuit is also 555 based, but is unique in that it arranges for the wipers to be activated immediately at power-on.

The circuit diagram of Fig. 1 shows the internal organization of the 555 timer to aid in clarifying the operation of the present circuit. When S1 is closed, pin 6 is immediately pulled to +12 V because C1 is discharged as yet (see also Fig. 2b). The bistable in the 555 is reset, the output goes low, and Re+ is energized. This forms the basic difference with the standard application of the 555, where C1, connected as shown in Fig. 2a, delays the relay action until charged to 2/3 of the supply voltage. Returning to Fig. 1, C1 is charged via R2 and the 555's internal transistor when the output is activated. The bistable is reset when the voltage at pin 2 drops below 1/3 Vcc, causing the relay to be de-energized, and C1 to be discharged via R1-P1. The dis-

1



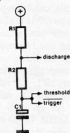
- 1 = GND
- 2 = trigger
- 3 = out
- 4 = reset
- 5 = control voltage
- 6 = threshold
- 7 = discharge
- 8 = Vcc

87508-1

charge time, and hence the wiper interval, is defined by the setting of P1. When this is set to the shortest delay, the wiper motor is constantly powered via Re, since C1 is not charged via P-R2 only, but effectively via voltage divider P-R1 also. The wiper delay is fed from the 12 V car battery, and its current consumption is practically that of the relay alone. Note that the coil current may not exceed 200 mA.

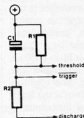
TW

2a



87508-2a

b



87508-2b

From an idea by C Trimbach

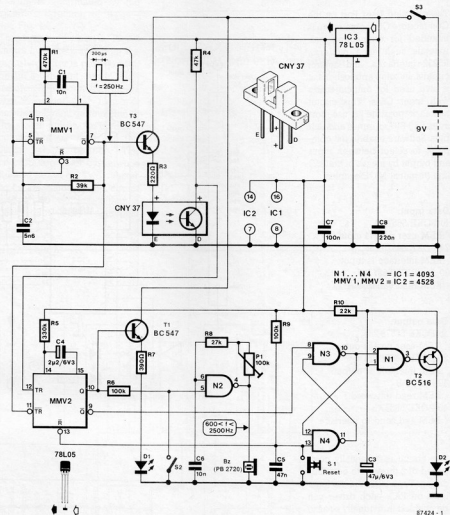
This circuit provides audible and visible warning when a fish is nibbling the bait. Although this event is fairly easy to signal with electronic means, the circuit is relatively extensive to ensure that it can be powered from a 9 V battery.

The circuit is based on a slotted opto-coupler Type CNY37, and a home made notched wheel. Unfortunately, the current amplification of slotted opto-couplers is very low (0.02 min.), requiring considerable current to be fed through the LED before a usable collector current flows in the phototransistor. To avoid rapidly exhausting the battery, MMV<sub>1</sub> pulses the LED at about 250 Hz and a duty factor of 0.05. MMV<sub>2</sub> detects the presence of these pulses.

When a fish pulls at the bait, the notched wheel revolves in the slot, and intermittent pulse bursts are received at the trigger input of MMV<sub>2</sub>. Green LED D<sub>1</sub> lights, buzzer Bz beeps, and bistable N<sub>1</sub>-N<sub>4</sub> is set, so that red LED D<sub>2</sub> flashes at a 1.5 Hz rate. D<sub>1</sub> and the buzzer are turned off when the fish gets off after nibbling the bait, but D<sub>2</sub> continues to flash. The circuit around N<sub>1</sub>, T<sub>2</sub> and C<sub>3</sub> then serves to keep the current consumption as low as possible. The circuit can be reset by pressing S<sub>1</sub>.

Preset P<sub>1</sub> enables adjusting the frequency of the buzzer oscillator between 600 and 2500 Hz. When several fishing-rods are being used, each can be assigned a particular signal tone. The buzzer can be switched off by means of S<sub>2</sub>.

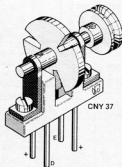
A suggested construction of the light barrier and the notched wheel is shown in Fig. 2. A small shaft is used in combination with a reel around which the fishing line revolves. The slots cut into the detection wheel should not be too wide: 1 mm is a good starting value.



The detection sensitivity is determined by the number of slots in combination with the reel diameter. The light barrier should be screened from daylight.

In the stand-by condition, the circuit consumes no more than 4 mA, which goes mainly on account of the LED in the opto-coupler. In the actuated state, the current consumption rises to about 12 mA.

TW



The so-called User Port on the Commodore C64 home micro is intended for connecting peripherals such as a modems, RS232 interfaces, and control circuits. In some applications, it is also used for communication with other C64s. This circuit makes it possible to use port lines PB0-PB7 as inputs and outputs. Software enables the computer to select between input and output by means of the PA2 line (terminal M). Examples:

## Data input:

```
10 POKE 56579,0
:REM user port is input.
20 POKE 56576,255
:REM interface is input.
30 A = PEEK(56577)
:REM read variable A.
```

## Data output:

```
10 POKE 56579,255
:REM user port is output.
20 POKE 56576,251
:REM interface is output.
30 INPUT B
:REM read dataword.
40 POKE 56577,B
:REM and send to interface.
```

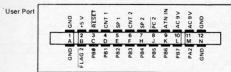
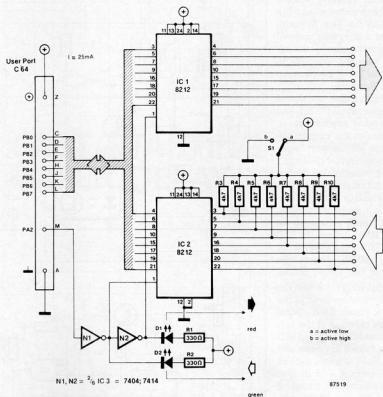
The circuit is essentially composed of 2 three-state octal bus drivers Type 8212. Via the logic level on PA2, each driver can be enabled individually so as to select between the input or output function of the interface, whose current state is indicated by a pair of LEDs. Switch S<sub>1</sub> selects between pull-up (a) or pull-down (b) termination of the input lines.

Finally, an example for interactive data processing:

```
10 POKE 56567,255
:REM interface is input.
20 POKE 56579,0
:REM user port is input.
30 A = 255-PEEK(56577)
:REM read variable A.
100
:REM example of logic control:
```

```
110 IF A=1 THEN B=64
111 IF A=2 THEN B=128
112 IF A=4 THEN B=192
113 IF A=8-1 THEN B=32
```

```
300 POKE 56577,B
:REM load data register
310 POKE 56579,255
:REM user port is output
320 POKE 56576,251
:REM interface is output
330 GOTO 10
```



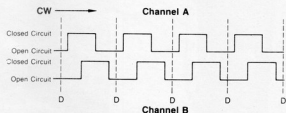
Industrial engineers and system operators need not be told of the often awkward problems that arise from having to change a thumbwheel setting. It is not surprising, therefore, that alternatives for the good old thumbwheel switch are currently finding their way in new designs. The present circuit was designed to work with the Type ECW1J-B24-AC0024 digital contact encoder from Bourns. This device looks very much like an ordinary potentiometer, but essentially contains two switches. These are normally opened, and successively closed when the spindle is

rotated one step. The order of closing is determined by the spindle's direction of travel—see Fig. 1.

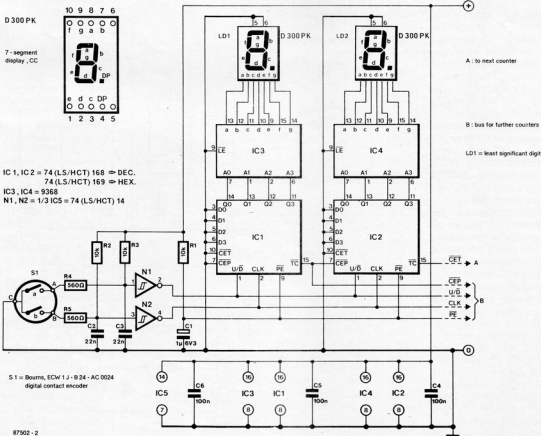
The circuit diagram in Fig. 2 shows how the signal from the digital encoder is processed to obtain a two-digit display indication. Two Schmitt triggers and associated R-C networks ensure sufficient debouncing of the switch pulses. An up/down counter keeps track of the actual switch position. The counters are reset by network R<sub>1</sub>-C<sub>1</sub> at power-on. Two counter types are stated in the circuit diagram to provide either a hexadecimal (0-FF) or a decimal

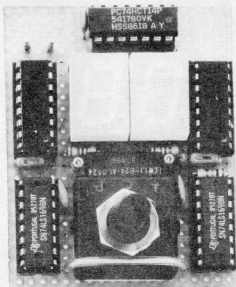
1

FULL CYCLE PER DETENT  
(Normally Open in Detent Shown)



2





(0-99) display. The displays and associated drivers can be omitted if the  $Q_1$ - $Q_2$  outputs on the counters are used to drive a computer input port direct. The maximum current consumption of the 2-digit version is about 400 mA, which goes mainly on account of the 7-segment displays. *TW*

Bourns Electronics Limited • Hodford House • 12/27 High Street • Houndslow • Middlesex TW3 1TE. Telephone: (01 572) 6531.

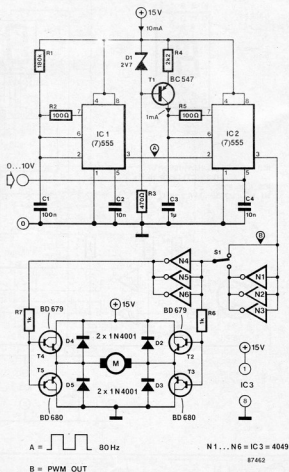
## 103

## PWM DRIVER FOR DC MOTORS

The speed of DC motors is relatively simple to control. For independently energized motors, the speed is, in principle, a linear function of the supply voltage. Motors with a permanent magnet are a sub-category of independently energized motors, and they are often used in toys and models. In this circuit, the motor supply voltage is varied by means of pulse width modulation (PWM), which ensures good efficiency as well as a relatively high torque at low motor speeds.

A single control voltage between 0 and +10 V enables the motor speed to be reversed and varied from nought to maximum in both directions. Astable multivibrator IC<sub>1</sub> is set up as an 80 Hz oscillator, and determines the frequency of the PWM signal. Current source T<sub>1</sub> charges C<sub>1</sub>. The sawtooth voltage across this capacitor is compared with the control voltage in IC<sub>2</sub>, which outputs the PWM signal to buffer N<sub>1</sub>-N<sub>2</sub> or N<sub>3</sub>-N<sub>6</sub>. The darlington-based motor driver is a bridge circuit capable of driving loads up to 4 A, provided the run-in current stays below 6 A, and sufficient cooling is provided for the power transistors T<sub>2</sub>-T<sub>5</sub>. Diodes D<sub>2</sub>-D<sub>5</sub> afford protection against

inductive surges from the motor winding. Switch S<sub>1</sub> makes it possible to reverse the motor direction instantly. *St*



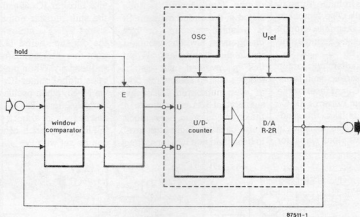


Conventional analogue sample and hold circuits are notorious for their tendency to drift, a phenomenon unknown in digital memories. It is, therefore, interesting to study the use of a digital memory element for storing an analogue signal.

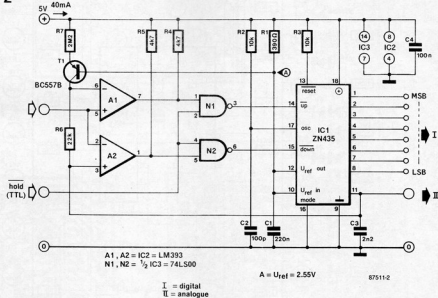
The present circuit is based on intermediate storage of digitized analogue information, and therefore requires an analogue-to-digital converter (ADC) at the input, and a digital-to-analogue converter (DAC) at the output. Unfortunately, DACs and ADCs are typically expensive components, and the present circuit is therefore set up with a DAC only, driven by an up/down counter—see Fig. 1. The counter is essentially an ADC, since the output voltage of the R-2R based DAC is continuously compared to the input voltage with the aid of a window comparator. The error signal produced by the comparator arranges for the counter to count up or down, depending on the magnitude of the difference between the input and output voltage. The up/down counter is corrected until the input and output voltage are equal. The digitized result of the A-D conversion is available at the counter outputs.

The extensions for converting the basic set-up into a sample & hold circuit are relatively simple. The current count is retained by activating the HOLD input, which enables halting the U/D counter. Evidently, the counter state is not subject to drift, so that the analogue output signal is available unaffected for as long as the circuit is powered. The converter used here is the Type ZN435 ADC/DAC from Ferranti. This chip contains everything shown in the dashed box of Fig. 1. With reference to the practical circuit diagram, Fig. 2, the internal voltage reference and the oscillator are adjusted with R<sub>1</sub>-C<sub>1</sub> and R<sub>2</sub>-C<sub>2</sub> respectively. The latter are dimensioned for 400 kHz, i.e., nearly the maximum oscillator operating frequency. The internal counter is controlled via inputs

1



2



up, down and mode. The logic level applied to the mode input determines whether the counter continues or halts upon reaching state 0 or the maximum value, 255. In the present application, the counter is halted. Gates N<sub>1</sub> and N<sub>2</sub> are added to enable blocking the U/D counter. Opamps A<sub>1</sub>, A<sub>2</sub> form the window comparator. Current source T<sub>1</sub>, R<sub>7</sub> and R<sub>6</sub>

arrange for the toggle threshold of A<sub>1</sub> to be 20 mV higher than that of A<sub>2</sub>. This off-set creates the window, or inactive span, needed to suppress oscillation of the counter's LS bit, and to prevent unwanted effects arising from the comparators' offset voltages. Decoupling capacitor C<sub>1</sub> is fitted for suppressing spikes that occur during state changes on the counter out-

puts. The conversion time of this design is about 640 μs, as determined by the oscillator frequency (400 kHz), the resolution (8 bits) and the input voltage change (2.55 V<sub>pp</sub> max.). This corresponds to a slow rate of 4 mV/μs at the input. Finally, bear in mind that the output impedance (IC<sub>1</sub> pin 11) is relatively high at about 4 kΩ. *TW*

This electronic version of the reversible sand-glass uses a set of LEDs to simulate the passing of sand grains from the upper to the lower bulb. The simple to build circuit is accurate enough for most domestic timing applications.

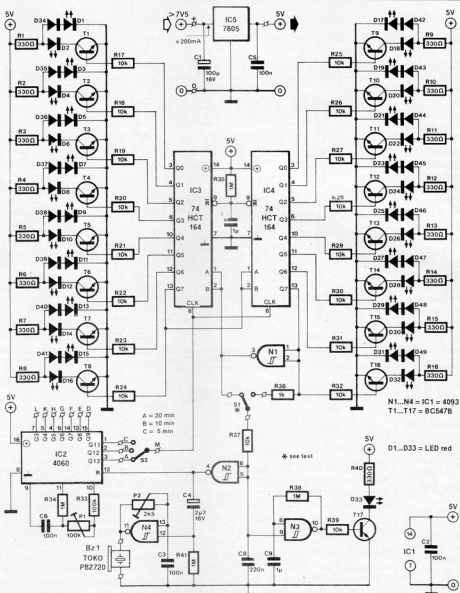
The circuit diagram appears in Fig. 1. On power-up, shift registers IC<sub>2</sub> and IC<sub>4</sub> are reset by the low pulse from network R<sub>35</sub>-C<sub>5</sub>. A few seconds later, the sand-glass is started. The oscillator in IC<sub>2</sub> generates a clock signal for

the shift registers. The clock frequency is adjustable with P<sub>1</sub>. Switch S<sub>1</sub> enables selecting one of the three timing periods stated in the circuit diagram. S<sub>1</sub> is a small mercury or ball changeover switch mounted inside the sand-glass. When this is reversed, the switch toggles and so selects the odd or even numbered LEDs. Assuming that S<sub>1</sub> is set as shown in the circuit diagram, every clock pulse causes a logic high level to be shifted into IC<sub>2</sub>, for as long

as pin 13 of IC<sub>2</sub> remains logic low. The MS bit of IC<sub>2</sub> (output Q7) is shifted into the second shift register, IC<sub>4</sub>. Controlled by the shift register outputs, transistors T<sub>1</sub>...T<sub>16</sub> incl. switch off the odd numbered LEDs, and light the even numbered ones sequentially. When pin 13 of IC<sub>2</sub> goes high, counter IC<sub>3</sub> is reset via N<sub>1</sub>-N<sub>2</sub>, while oscillator N<sub>4</sub> is started. Buzzer Bz<sub>1</sub> is actuated and sounds for about 2 seconds (C<sub>4</sub>+R<sub>4</sub>). The pitch of the tone can be set with P<sub>2</sub>.

When the sand-glass is reversed, S<sub>1</sub> toggles, ending the reset state of IC<sub>2</sub>. Logic low levels are shifted into IC<sub>2</sub> because pin 13 of IC<sub>2</sub> is logic high. The even numbered LEDs are extinguished one by one, and the odd numbered ones are illuminated, until pin 13 of IC<sub>2</sub> goes low again. IC<sub>2</sub> is reset, Bz<sub>1</sub> produces a short beep, and the sand-glass can be reversed for a new timing period. LED D<sub>33</sub> indicates that the sand-glass is operative. The circuit is fed

1



Resistors ( $\pm 5\%$ ):

R<sub>1</sub>...R<sub>16</sub> incl.; R<sub>40</sub> = 330R  
 R<sub>17</sub>...R<sub>32</sub> incl.; R<sub>37</sub>; R<sub>39</sub> = 10K  
 R<sub>33</sub> = 100K  
 R<sub>34</sub>; R<sub>35</sub>; R<sub>36</sub>; R<sub>41</sub> = 1MΩ  
 R<sub>38</sub> = 1KΩ  
 P<sub>1</sub> = 100K preset  
 P<sub>2</sub> = 2K5 or 2K2 preset

## Capacitors:

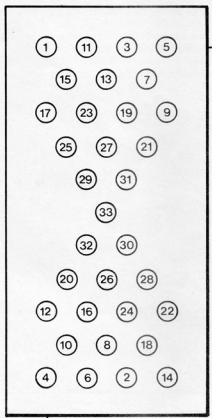
C<sub>1</sub> = 100μF; 16 V; axial  
 C<sub>2</sub>; C<sub>3</sub>; C<sub>4</sub>; C<sub>5</sub> = 100n  
 C<sub>6</sub> = 2μF; 16 V; radial  
 C<sub>7</sub>; C<sub>8</sub> = 1μF  
 C<sub>9</sub> = 220n

## Semiconductors:

D<sub>1</sub>...D<sub>33</sub> incl. = red LED  
 D<sub>34</sub>...D<sub>48</sub> incl. = 1N4148  
 T<sub>1</sub>...T<sub>17</sub> incl. = BC547  
 IC<sub>1</sub> = 4093  
 IC<sub>2</sub> = 4060  
 IC<sub>3</sub>; IC<sub>4</sub> = 74HCT164  
 IC<sub>5</sub> = 7805

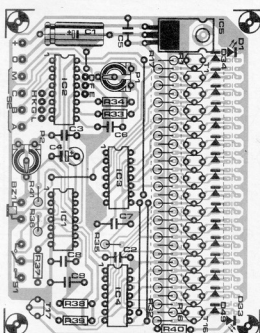
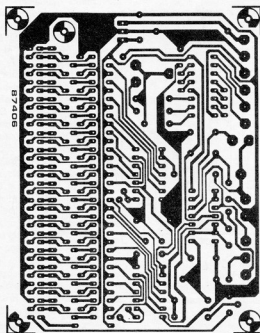
## Miscellaneous:

B<sub>21</sub> = PB2720 (Toko; Cirkit stock no. 43-27201).  
 S<sub>1</sub> = SPDT mercury, ball or tilt switch, e.g. Maplin order no. FE11M, or ElectroValue no. 339-881.  
 S<sub>2</sub> = single-pole, 3-position rotary switch plus knob.  
 PCB Type 87406 (available through the Readers Services).  
 Suitable ABS enclosure.  
 DC power socket.



87406-2

from a small mains adaptor capable of supplying about 200 mA at an output voltage between 7.5 and 12 VDC. Construction of the sand-glass is straight-forward using PCB Type 87406—see Fig. 2. The position of the LEDs on the front panel of the enclosure is shown in Fig. 3. Make sure that each LED is connected to the corresponding soldering island on the PCB. SPDT Switch S<sub>1</sub> is made from two SPST mercury or ball switches, fitted together but mutually reversed at a suitable position in the enclosure. The action of the switches is tested by reversing the sand-glass and measuring the switch configuration with the aid of a continuity tester or an ohm meter. All parts in the sand-glass enclosure should be fitted securely in view of the reversibility of the enclosure. The socket for connecting the adaptor, and rotary switch S<sub>2</sub>, are fitted in one of the side panels. A prototype of the electronic sand-glass is shown in Fig. 4. The detachable front panel that holds the LEDs was cut from perspex sheet. R



## DIVIDER CASCADE



This circuit can be driven either with an analogue, or a digital, precision 10 MHz signal for dividing down to a number of commonly used timebase periods. The oscillator proposed in [1] is particularly suitable for driving the present cascade, since it offers excellent stability thanks to the use of a 10 MHz quartz crystal fitted in an electronically controlled oven. It should be noted, however, that its output is digitally compatible, so that components R1-C1 and R2 at the input of the circuit shown here can be omitted, i.e., N1 is driven direct. Where an analogue, sinusoidal, 10 MHz signal is used, the amplitude must be 750 mV<sub>rms</sub>. Evidently, R1-C1 and R2 are then required to make the signal digitally compatible for clocking IC3. The circuit diagram shows that the cascade can be extended by adding further 74HC(T)390s and pairs of bistables. The Type 74HC(T)390 (IC3) holds two counters, the first of which divides by two (1QA), and by 5 (1QC). Bistable FF1 is driven with the 1QD output, and out-

puts the :10 signal, which is also applied to the CLK inputs of the second counter in IC3. This also divides by 2 and 5, while FF2 gives a total division factor of 100 in the first block of the cascade. The use of decade counters results in output periods commonly used for an oscilloscope timebase. Counters and bistables may be added to obtain relatively long, yet accurately defined, periods for specific applications. The current consumption of the circuit as shown is about 12 mA. With two divider blocks added,

the total current drain is expected to be approximately 25 mA, not 36 mA, since HCMOS circuits require less power at lower clock frequencies.

D

#### Reference:

[1] *Oven-compensated oscillator*. Elektor Electronics, January 1986.

## 107

## FORCED COOLING FOR REFRIGERATOR

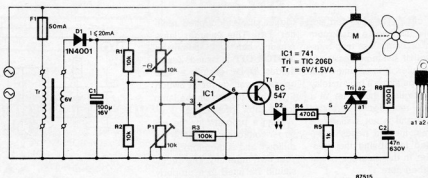
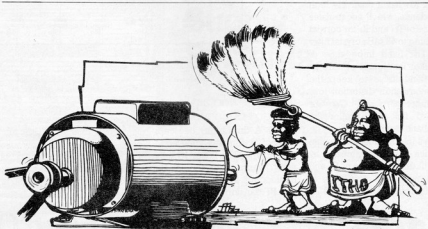
Refrigerators dissipate the heat extracted from the inside via a grid structure mounted at the rear side. When a refrigerator is located in a confined space, the rear side can get fairly hot owing to the limited convection. This problem derates the overall efficiency of the refrigerator, since the motor is automatically switched on for longer periods when a considerable difference exists between the inside and outside temperature—notably on hot days it often seems as if the motor is running continuously. The ventilation control described here can help economize on power consumption. The circuit is simple, and does not require a detailed description. A simple DC supply is set up with Tr-D1-C1. Temperature is measured with the aid of bridge circuit R1-R2-P1, and a NTC (negative temperature coefficient resistor). IC1 is a comparator which converts the bridge output into a gate current for triac Tr1, which controls extractor fan M. Some hysteresis is provided by feedback resistor R3. The triac is controlled with a direct gate current to avoid triggering problems arising from induced voltage peaks.

The circuit is uncritical as regards construction. Be sure to observe the correct connection of the a1 and a2 terminals on the TIC206, else it remains trig-

gered permanently. It should be noted that the circuit is dangerous to touch, as it is connected direct to the mains. It is possible to reduce the stand-by

current by omitting Tr1, and powering the circuit in parallel with the refrigerator motor. The NTC should be fitted near the grid at the rear side of the

refrigerator. The triac can do without a heat-sink. TW



87515

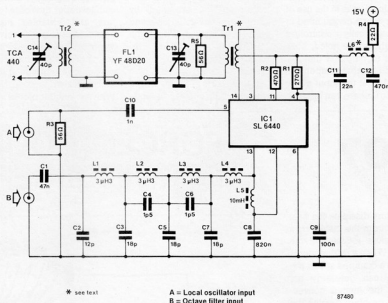
There are many conflicting technical requirements for a good-quality front-end in an SW receiver. The noise figure and the intermodulation level should be low, the RF insulation between ports LO, RF and IF should be high, and some amplification is desirable. The Type SL6440 high level RF mixer from Plessey ensures a noise figure of around 10 dB, and offers sufficient suppression of the LO signal. The signal applied to the RF input (B) of the front-end is passed through a low-pass filter with a cut-off frequency of 32 MHz and an output impedance of 500  $\Omega$ . The open collector output of mixer IC<sub>1</sub> has a relatively high impedance, which necessitates the use of Tr<sub>1</sub> and R<sub>3</sub> for correct matching to 48 MHz crystal filter FL<sub>1</sub>. The fixed impedance of this filter for signals outside its pass-band helps to keep the intermodulation distortion low. Trimmers C<sub>13</sub> and C<sub>14</sub> are aligned for a maximum flat pass-band at minimum loss. The mixer's intermodulation characteristics can be optimized by careful dimensioning of R<sub>1</sub> and R<sub>2</sub>, provided the amplitude of the local oscillator signal is

stable. A third-order intercept point of 33 dBm was achieved in a prototype. The mixer IC gets fairly warm, and should be cooled with a heat-sink. The RF transformers are wound

as follows (use 30SWG enamelled wire):

Tr<sub>1</sub>: the primary winding is 10+10 bifilar turns, the secondary is 10 turns, on a Type T50-12 ferrite core.

Tr<sub>2</sub>: the primary winding is 2 turns, the secondary 18 turns, on a Type T50-12 ferrite core. L<sub>6</sub>: 6 turns through a ferrite bead.



\* see text

A = Local oscillator input  
B = Octave filter input

97400

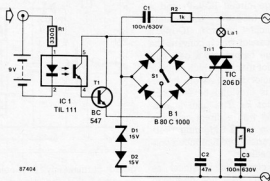
This circuit is intended for anyone lacking a darkroom timer, or being less than satisfied with it, but in possession of a computer. It is assumed that the computer has a built-in relay for controlling the motor in a cassette recorder. Where this relay output is not available, a different method needs to be adopted for driving the opto-coupler in the enlarger circuit described here.

An MSX computer can actuate the relay in question with the aid of BASIC command **MOTOR ON**. This causes the phototransistor in opto-coupler IC<sub>1</sub> to conduct, so that T<sub>1</sub> can

trigger silicon-controlled rectifier Tr<sub>1</sub>. The enlarger lamp remains on until command **MOTOR OFF** is issued. Zener diodes D<sub>1</sub>-D<sub>2</sub> ensure a safe operating voltage for T<sub>1</sub>. Switch S<sub>1</sub> enables turning on the lamp for position adjustments.

Writing a program for the enlarger control should not be too difficult, and is therefore left to your own ingenuity. The circuit should be fitted in a properly earthed metal case or an ABS enclosure to prevent accidental contact with points at mains potential.

R



97404

# NEW PRODUCTS • NEW PRODUCTS • NEW

## MULTIPOINT SCANNER

Multipoint Process Scanners are a logical extension of the Series 4500 high precision 4 1/2 digit Process Monitors.

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The AUTOSCAN is supported by a wide range of options and accessories that include PT-100/Thermocouple linearization and selectable digit alarms with two or more setpoints per channel.



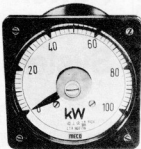
For further information please contact:

**ACCORD ELECTRONICS**  
201 Yashodham Enclave  
SA-1/56, Goregaon Mulund  
Link Road, Goregaon (East)  
Bombay 400 063.

## PANEL METERS

In addition to their existing range of DIN size 72mm, 96mm and 144mm Square 240° Circular Scale Indicating Panemeters, MECO have now introduced another 240°

Circular Scale Panel Meters with a clear transparent Acrylic Square front of 110 x 110mm and a round Phenolic moulded body of 100mm diameter. Ammeters & Voltmeters (both AC as well as DC) Frequency Meters, Wattmeters, Power Factor Meters & VAR Meters are available in the above Model. The above instruments have been developed primarily for defence use. These instruments are mainly used in the control panels installed in Power Stations.



For further information please contact:

**MECO INSTRUMENTS PVT. LTD.**  
Bharat Industrial Estate  
T.J. Road, Sewree  
Bombay 400 015  
Phone No.: 4137423  
4132435, 4137253  
Telex: 11 71001 MECO IN  
Cable: STANCOR  
Bombay 15.

## TOOL KIT

This is a new double zipped, padded wallet which contains a range of electronic aids to handle various jobs. The wallet has 23 fitted pouches to hold the items securely. The kit includes light weight cushion gripped IC cutter, Flat Nose Plier, Micro probes-minipulators, Desoldering gun, knife with 4 replaceable blades of different designs, Tong, Claw, Fibre grip heat resistant device, heat shunt, Component handling

tweezer, Triangular file, PCB Brush, Hand held drill, Wire Stripper, Pin Vice, Doofer, Magnifying glass, Scissor, Retrieval Device and IC Insertion And Extraction device.

External dimension of the wallet when closed are: 12" x 9" x 1 1/2" and weighs 850gms only.



For further information please contact:

**KOHLI TECOMA**  
Stereo House, 46, 1st Marine  
Street, Dhobitalao  
Bombay 400 002. (India)  
Phone No.: 319128, 8121167.

## MILLI-OHM METER

The VRM22M with its four terminal measurements and 0.1 milli ohm resolution, makes low resistance measurement very simple and accurate. Being BATTERY/MAINS operated and light



weight it can be carried to the work spot. VRM22M has 3 1/2 digit 0.5 inch bright LED display which is ideal for both factories and labs. In most cases it replaces the KELVIN DOUBLE BRIDGE.

For further details please contact:

**VASAVI ELECTRONICS**  
(Marketing Division)  
630 Alkarim Trade Centre  
Ranigani  
Secunderabad 500 003.  
Phone No: 70995.

## MULTIMETER

**LEDTRON ELECTRONICS** has introduced Pocket size analog Multimeter model 1015B in association with M/s. Hung Chang Products, Korea. It can measure DC/AC voltage upto 1000V DC current upto 250MA, Resistance upto 10 Megohm, decible from -20 db to 62 db and battery check for 1.5V and 9V batteries. Other features are a 10000 Ohms/VDC sensitivity and 90° Arc mirrored scale for accurate reading.



For further information please contact:

**LEDTRON ELECTRONICS**  
170 Lohar Chawl  
Bombay 400 002.

# NEW PRODUCTS • NEW PRODUCTS • NEW

## DATA SCANNER

Advani-Oerlikon have developed a mini microprocess-based data scanner called UDS-30. This 30-point scanner is designed for scanning of temperature, voltage or any other parameters of water and steam boilers, windings of HP motors and high voltage transformers, distribution points in silos containing foodgrains, engine test and reaction vessels in chemicals and process industries.

The system is field proven, versatile and compact. It is mounted in a standard RA 19 rack. It can accept multi-variable inputs such as Thermocouples, RTDs and Analogues. The system has built-in 24 columns, an alphanumeric 2 colour printer with re-rolling facility which gives out print out of scanned data and programmed parameters. The keyboard functions such as low level set point, control level set points, dwell time, high level set point, channel number, hysteresis, etc. are programmable individually for each channel. Display annunciation is provided for each channel. There are totally 90 LEDs. Each channel has a separate indication for alarm, sensor break and control status. The system also has the facility to scan alarm conditions on a priority basis. Output relay contacts are provided for each channel. One relay is provided for common alarm and one for sensor break indication. EEPROM memory is used and hence no battery back up is required for the programme. A real time calendar is also provided which gives date, month, year, day of the week and time. Nickel cadmium battery is provided for the back-up of the calendar. The system uses a floating point arithmetics for linearisation

and other mechanical calculations.

Solid-state semiconductor switches are used for multiplexing, thus contributing to reliability and compactness. STD cards are used for flexibility of operation and ease of maintenance, thus ensuring minimal downtime. The plug-in PCB and the STD mother board have minimised wiring in the instrument. The unit has a hinged transparent unbreakable cover on the front space to avoid any accidental changes in the keyboard function.



For further information, quote ref: PUB/2, contact: ADVANI-OERLIKON LIMITED Post Box No. 1546 Bombay 400 001

## SPECTRUM ANALYSER

ROFIN-SINAR LASER UK LTD, announce the introduction of the high speed RSO 6240 Spectral Processor to operate with the current line of Optical Spectrum Analyser equipment. The new instrument includes a more powerful processor, together with many system improvements such as dual double-density double-sided 3 1/2" disc drives, an improved monitor, and digitising electronics.

The entire system has been repackaged with an integral keyboard instead of the earlier separate keyboard. In addition various accessories and software packages have been added to provide a very

powerful package to measure transmission, absorption, reflection and colour, in addition spectroradiometric and software package. The system captures a complete spectrum in 5 msec and stores it in 80 msec in the processor. The wavelength range is 200-5000 nm which can be covered at one time using the "merge" software facility.



For further information, contact: TOSHNI-TEK INTERNATIONAL 267 Kilpauk Garden Road Madras 600 010.

## THERMOCOUPLE VACUUM METER

The IBP Thermocouple Vacuum Meter is a simple, single head measuring device.

### SPECIFICATIONS

Gauge Head: Chromium plated brass with octal socket. Vacuum Connections: Through standard 6 mm screwed union. Measuring Range: 1-1000 Microns. Calibration: Calibrated for dry air using a McLeod gauge. Power Supply: 230 Volts, 50 Hertz,  $\pm 10\%$ . Dimensions: Small, compact construction with simple panel installation in Standard half module (H 135 mm x W 210 mm x D 145mm). Standard accessories supplied: Gauge head with cable of length 3 Metres. Applications: Used in Industrial Systems, Refrigeration Industry, Flask, Lamps, Capacitors and Condenser Industries etc.



For further information please contact:

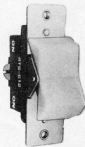
IBP CO. LIMITED A Govt. of India Enterprise Engineering Division Sewri (East) Bombay 400 015.

## "ROCKER TOGGLE" SWITCH

IEC has just introduced a range of "Rocker Toggle" switches with Black, Red, Blue, White, Yellow or Green colour knobs.

These Rocker Toggle switches are available in 6A, 10A, 15A, 250V AC or 28V DC in single and double pole with on-off, changeover with or without centre off and momentary contact, to serve as Push Button. Special circuits are possible e.g. 1,2,3 or 1, 1+2, 2+3, etc., avoiding the need of 2 or 3 switches.

Switches are supplied with screw terminals or push-in terminals (6.3mm).



For further information please contact:

INDIAN ENGINEERING COMPANY Post Box 16551, Worli Naka Bombay 400 018.



# LUXCO<sup>®</sup>

## COLOUR TV SPEAKERS



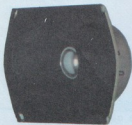
10 LFCT 5



6-9 LCT 3



8-13 LCT 5



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5 LT 10



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7 LDT 10 S

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8. TBA 810-7W+7W Stereo Amp	8-00	60-00
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10. TBA 810-7W with Vol. Bass, Treble	6-00	70-00
11. TBA 810-7W+7W with Vol. Bass, Treble	12-00	140-00
12. TBA 810-7W+7W Stereo Amp with 741 Control Amp.	22-00	200-00
13. Philips Hifi 8W Amp.	12-00	110-00
14. Philips Hifi 15W Amp.	10-00	125-00
15. Philips Hifi 25W Amp.	10-50	135-00
16. Philips Hifi 40W Amp.	7-00	150-00
17. TDA 1010 10W Mono Amp.	3-00	45-00
18. TDA 1010 (10W+10W) Stereo Amp.	6-00	90-00
19. TDA 2020 20W Mono Amp. (Single Supply)	8-25	95-00
20. TDA 2020 (20W+20W) Stereo Amp. (Single Supply)	16-50	190-00
21. TDA 2020 20W Mono Amp. (Dual Supply)	8-50	85-00
22. TDA 2020 (20W+20W) Stereo Amp. (Dual Supply)	17-00	170-00
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7. Electronic Dog	7-00	170-00
8. 12 Tune Car Reverse Horn	4-00	60-00
9. Scooter Brake Horn	3-00	50-00

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	PCB PRICE	KITS PRICE
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2. 78 L General Power Supply	2-50	30-00
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