CONTENTS

SAFETY INSTRUCTIONS

SAFETY - PRECAUTIONS
WARNING: The following precautions should be observed.

1. Although the chassis is isolated from the mains supply, some areas of the main PCB are at mains potential. An isolation transformer (250-500 VA) should therefore be connected between the mains and the receiver before service is attempted.

2. Do not install, remove, or handle the picture tube in any manner unless safety goggles are worn. People not equipped should be kept away while picture tubes are handled. Keep the picture tube away from the body while handling.

3. When replacing the chassis in the cabinet, ensure all the protective devices are put back in place, such as: barriers, non-metallic knobs, cable ties, adjustments and compartment cover or shields, isolation resistor-capacitor, etc.

4. When service is required note the original lead locations and anchor points. Ensure all leads, especially in areas of high voltage, are routed/anchored in their correct locations when reassembling the receiver.

5. Always use the manufacturer's replacement safety component. Always replace original spacers and maintain lead lengths. Critical safety components should not be replaced by other makes. Furthermore where a short circuit has occurred, replace those components that indicate evidence of overheating.

6. Before returning a serviced receiver to the customer, the service technician must throughly test the unit to be certain that it is completely safe to operate without danger of electric shock, and be sure that no protective device built into the instrument by the manufacturer has become defective, or inadvertently damaged during servicing. Therefore, the following checks are recommended for the continued protection of customers and service technicians.

INSULATION
Insulation resistance should not be less than 10M at 500V DC between the mains poles and any accessible metal parts.
Also, no flashover or breakdown should occur during the dielectric strength test applying 3kV AC or 4.25kV DC for two seconds between the mains poles and accessible metal parts.

HIGH VOLTAGE
High voltage should always be kept at rated value of the chassis and not higher. Operating at higher voltage may cause a failure of the picture tube or high voltage supply and also, under certain circumstances could produce x-ray radiation moderately in excess of design levels. The high voltage must not, under any circumstances exceed 26kV on the chassis.

X-RAY RADIATION
TUBES: The primary source of x-ray radiation in this receiver is the picture tube. The tube utilised for the above mentioned function in this chassis is specially constructed to limit x–ray radiation. For continued x-ray radiation protection, replace tube with the same type as the original BEKO approved type.

PRODUCT SAFETY NOTICE
Many electrical and mechanical parts in television receivers have special safety related characteristics. These characteristics are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified by marking with a ⚠ on the schematics and replacement parts list in this Service Manual.
The use of substitute replacement components which do not have the same safety characteristics as recommended parts, may create electric shock, fire, X-ray radiation, or other hazards.

TUBE DISCHARGE
The line output stage can develop voltages in excess of 25kV; if removal of the EHT cap is required then, discharge the anode cap to chassis via a high value resistor, prior to its removal from the tube.

TECHNICAL SPECIFICATIONS 12.1 CHASSIS

1. OPERATING CONDITIONS

POWER SUPPLY	140 TO 270 VAC
NOMINAL OPERATING VOLTAGE	230 VAC
FREQUENCY	50 Hz
TEMPERATURE RANGE	0 TO 45 DEGREES C
HUMIDITY RANGE	YEAR'S MEAN = 75%
	MAX= 95%

2. RF SECTION

2.1 RECEIVING CHANNELS FOR VHF/UHF BAND

	CCIR	UK	FRANCE	OIRT
	B/G	I	L	D/K
VHF BAND				
BAND I	CHANNEL 2-4	CHANNEL2-5	CHANNEL 2-4	CH 1-5
BAND III	CHANNEL 5-12	CHANNEL 6-12	CH 5-12	CH6-12
CABLE	S1-S19,S20-S41	S1-S19,S20-S41	S1-S16, S21-S41	S1-S19-S22-S341
UHF BAND				
BAND IV-V	CHANNEL 21-69	CHANNEL 21-69	CH 21-69	CH 21-69

	MIN	NOM	MAX	UNIT
GAIN LIMITED SENSITIVITY				
INPUT SIGNAL LEVEL FOR				
STANDARD VIDEO OUTPUT VOLTAGE				
BAND 1/3	–	20	–	dB µV
BAND 4/5	–	23	–	dB µV
NOISE LIMITED SENSITIVITY				
INPUT SIGNAL LEVEL FOR 30 dB				
(S+N)/N-RATIO, WEIGHTED, CCIR				
REC 567				
BAND 1/3/4/5 :	–	30	–	dB (µV)

SELECTIVITY HF+IF

IF FREQUENCIES :

	B/G	I	L/L'	D/K
Picture Carrier	38.9	38.,9	38,9 / 33,9	38,9
Sound Carrier	33.4	32,9	32,4 / 40,4	32,4
Colour Carrier	34,47	34,47	34,5 / 38.3	34.5

VOLTAGE STANDING WAVE RATIO :	MIN	NOM	MAX	UNIT
BAND 1/3 :	–	2	4	–
BAND 4/ 5 :	–	2	4	–

MAXIMUM INPUT SIGNAL LEVEL :

BAND 1/3 : 100 dB µV (MAX)

BAND 4/ : 100 dB µV (MAX)

3. VIDEO OUTPUT SECTION

	MIN	NOM	MAX	UNIT
VIDEO OUTPUT VOLTAGE :				
(measured on cathode with				
lowest output level, contrast				
control and drive control at max :	90	100	–	V
FREQUENCY RESPONSE :				
INPUT AERIAL STANDARD, HF SIGNAL :				
STANDARD B/G - D/K-I-L :	–10		–7	– dB
INPUT: SCART PIN 20				
STANDARD B/G - D/K-I-L :			–8	–6 dB

4. CHROMA SECTION

		MIN	NOM	MAX	UNIT
PAL/SECAM					
COLOUR CAPTURE RANGE	:	+300/-500	±700	–	HZ
PHASE ERROR OF REFERENCE CARRIER	:	–	+–5	10	DEGRESS
COLOUR KILLER	:	30			dB µV (NOMINAL)

5. SOUND SECTION

		MIN	NOM	MAX	UNIT
SCART OUTPUT S/N RATIO	:	40	45	–	dB

NOISE LIMITED SENSITIVITY : 38 db/V (NOMINAL)
AM SUPRESSION RATIO : 60 db (NOMINAL)
POWER OUTPUT (at 10% distortion) fm= 1KHz : 2 W Rms 14"
2,5 W Rms 20"/21"

6. SYNCHRONISATION

LINE FREQUENCY LOCKING RANGE : ±700 HZ
VERTICAL FREQUENCY LOCKING RANGE : ±10 HZ

7. PICTURE TUBE DRIVE SECTION

EHT : 14": 23 KV±0,5 KV, 20"/21": 25,5 KV±0,5 KV

FOCUS VOLTAGE : MIN 25.6%
MAX 38%

GRID 2 VOLTAGE RANGE : MIN 0V, MAX 1400 V
HEATER VOLTAGE : 6.3±0.2 Vms

Power Supply Voltages

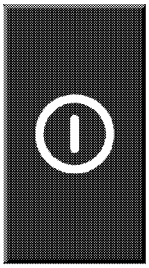
B+SUPPLY VOLTAGE (AT Ib=0)	14"	SS CPT	108V±1V
		LG CPT	104V±1V
		PH CPT	107V±1V
		IRICO CPT	113V±1V
	20"	SS CPT	121V±1V
		LG CPT	117V±1V
	21"	SS CPT	119V±1V
		LG CPT	113V±1V
13V OUTPUT Audio Mono			13±0.5 VDC
9V OUTPUT			9,0±0.5 VDC
5V OUTPUT			5.0±0.5 VDC

8. OTHERS

AMBIENT OPERATING TEMPERATURE : 0-45 DEGREES C
STORAGE TEMPERATURE : -10 TO + 85 DEGREES C
POWER CONSUMPTION 14" : 65 Watts (max)
20"/21" Mono Models : 85 Watts (max)

STAND-BY POWER : 5 Watts (max)
SAFETY : IEC 65 /BS P2N
X-RAY RADIATION : ACC. IEC 65 /BS P2N
Picture Tube Dimensions/Visible Screen Size : 14" (37 cm/34 cm)
20" (51 cm/48 cm)
21" (55 cm/51 cm)

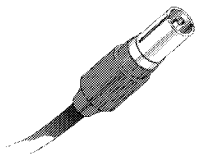
PREPARATIONS (Connections)



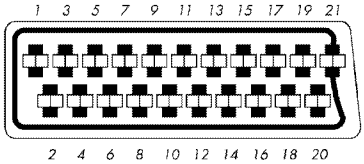
Connect the TV mains plug into your domestic mains socket outlet (230V 50Hz AC.)
To switch on press the TV on/off switch then any numbered button on the remote handset or P+/P– button on the control panel.

AERIAL CONNECTION

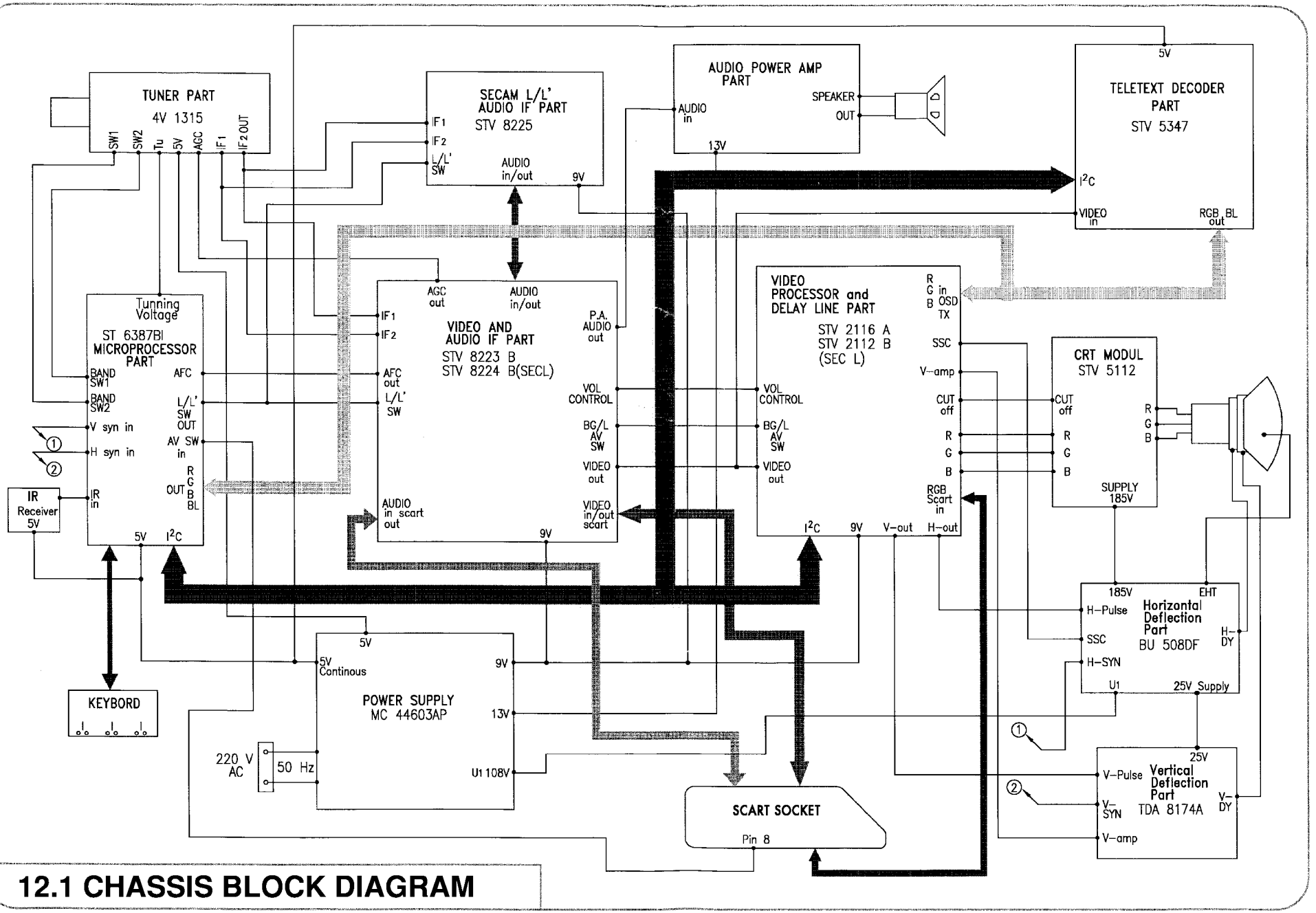
Using a 75 Ω aerial lead connect your TV to the aerial outlet in your home.



Pin Connections For Scart Socket



1- Audio output Right
2- Audio input Right
3- Audio output Left (Mono)
4- Audio ground
5- Blue ground
6- Audio input Left (Mono)
7- RGB input, Blue
8- Switching voltage
9- Green ground
10-
11. RGB input, Green
12.
13. Red ground
14. Ground
15. RGB input, Red
16. Blanking Signal
17. Video output ground
18. Video input ground
19. Video output
20. Video input
21. Screening



12.1 CHASSIS BLOCK DIAGRAM

Switch Mode Power Supply.

1. Primary

Mains is fed from the on/off switch (SW901), through the line filter circuit (L901, C901, C902) and then rectified to +330V by the bridge rectifiers (D901, D902, D903, D904). The initial start up voltage for pin 2 of IC901 is fed from R910. This thermistor goes high in value once the internal oscillator starts in IC901.
Pin 5 of TR901 supplies 12V to pins 1 and 2 of IC901 via L902, D906, R912.
The oscillator frequency (70-71 Hz*) from pin 3 of IC901 is fed to gate of T901.
The power supply will now start oscillating to produce the secondary voltages. D905, R903 and C906 are used to protect T901 and TR901 under fault conditions.

*** Note: During stand by the switching frequency is at 35Hz.**

2. Secondary

Secondary voltages +B✣, +5VA, +13V, and G1✣ are present in stand by mode as well as when the TV is powered up.
When the TV is switched out of standby pin 37 of IC401 goes high to supply the switching voltage for IC951.
IC951 supplies +9V to the base of T950 via R957. T950 is then biased on to give the +5VB supply and the will switch out standby.

✣ Note: The +B rail and G1 voltages are dependent on CRT size and type.

MC44603

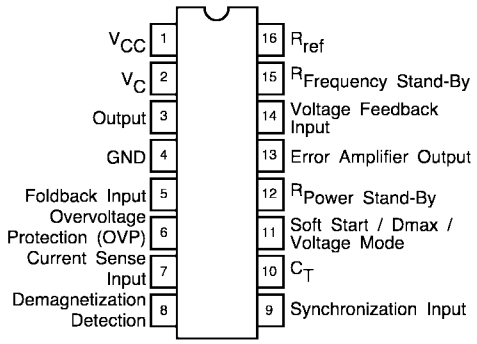
MIXED FREQUENCY MODE GREENLINE™ PWM CONTROLLER

Current or Voltage Mode Controller
- Operating up to 250 kHz Output Switching Frequency
- Inherent Feed Forward Compensation
- Latching PWM for Cycle-by-Cycle Current Limiting
- Oscillator with Precise Frequency Control

High Flexibility
- Externally Programmable Reference Current
- Secondary or Primary Sensing
- Synchronization Facility
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis

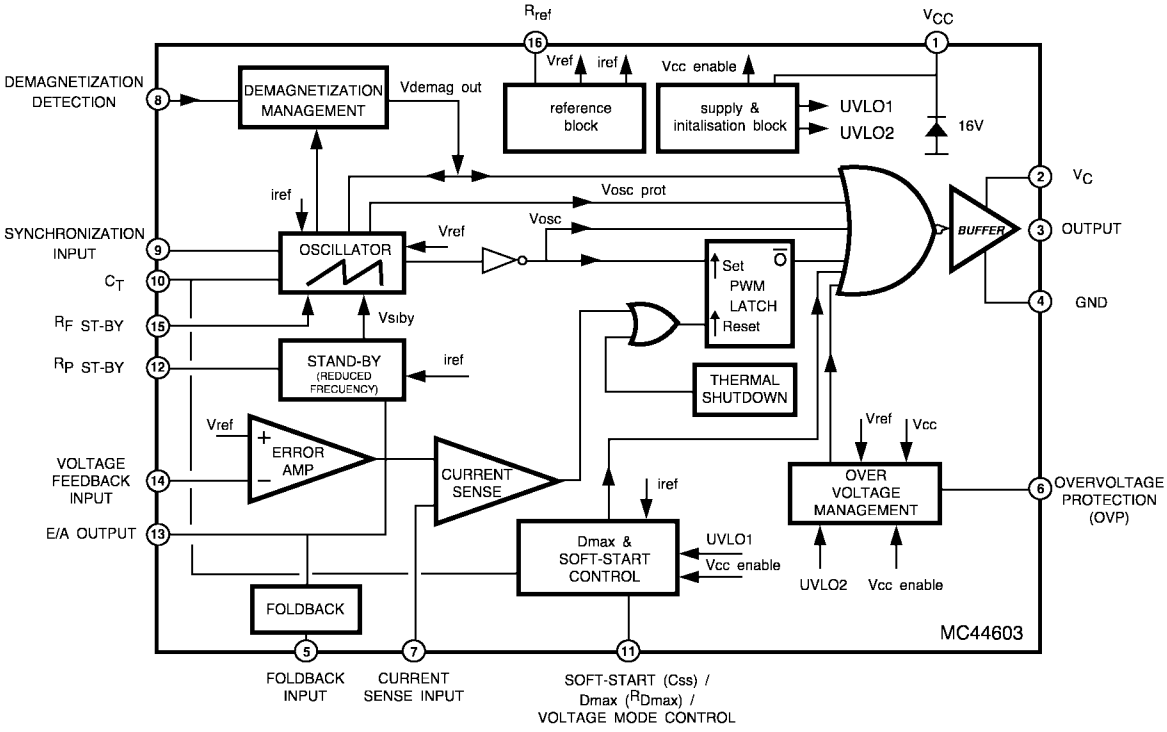
Safety / Protection Features
- Overvoltage Protection Facility against Open Current and Open Voltage Loop
- Protection against short Circuit on Oscillator Pin
- Fully Programmable Foldback
- Soft-Start Feature
- Accurate max Duty Cycle Setting
- Demagnetization (Zero Current Detection) Protection
- Internally Trimmed Reference

PIN CONNECTIONS



GreenLine™ Controller: Low Power Consumption in Stand By Mode
- Low Start-Up and Operating Current
- Fully Programmable Stand By Mode
- Controlled Frequency Reduction in Stand By Mode
- Low dV/dT for Low EMI Radiations

BLOCK DIAGRAM



PIN DESCRIPTION

PIN N°	NAME	PIN DESCRIPTION
1	V_{CC}	This pin is the positive supply of the IC. The operating voltage range after start-up is 9 V to 14.5 V
2	V_C	The output high state, Voh, is set by the voltage applied to this pin. With a separate connection to the power source, it gives the possibility to set by means of an external resistor the output source current at a different value than the sink current.
3	OUTPUT	The output current capability is suited for driving a power MOSFET, A Bipolar transistor can also be driven for low power applications. The maximum ON-time of the duty cycle can last up to %80 of the switching period.
4	GND	The ground pin is a single return typically connected back to the power source, it is used as control and power ground.
5	FOLDBACK INPUT	The foldback function ensures an overload protection. Feeding the foldback input with a portion of the V_{CC} voltage (1V max) establishes on the system control loop a foldback characteristic allowing a smoother start-up and a sharper overload protection. The foldback action performs an active current sense clamping reduction. Above 1 V the foldback input is no more active.
6	OVERVOLTAGE PROTECTION	When the overvoltage protection pin receives a voltages greater than 17 V the device gets disabled and requires a complete restart sequence. The overvoltage level is programmable.
7	CURRENT SENSE INPUT	A voltage proportional to the current flowing into the power switch is connected to this input. The PWM latch uses this information to terminate the conduction of the output buffer when working in current mode of operation. A maximum level of 1 V allows to limit the inductor current either in current or voltage mode of operation.
8	DEMAGNETIZATION DETECTION	A voltage delivered by an auxiliary transformer winding provides to the demagnetization pin an indication of the magnetization state of the flyback energy reservoir. A zero voltage detection corresponds to a complete core demagnetization. The demagnetization detection ensures a discontinuous mode of operation. This function can be inhibited by connecting Pin8 to GND.
9	SYNCHRONIZATION INPUT	The synchronization input pin can be activated with either a negative pulse going from a level between 0.7V and 0.3V to GND or a positive pulse going from a level between 0.7 V and 3.7 V up to a level higher than 3.7 V. Thus, it allows the next switching period to restart. The oscillator is free when connecting Pin9 to GND.
10	C_T	The normal mode oscillator frequency is programmed by the capacitor C_T choice together with the R_{ref} resistance value. C_T, connected between pin 10 and GND, generates the oscillator sawtooth.
11	SOFT-START/ D_{MAX}/ VOLTAGE-MODE	A capacitor or a resistor or a voltage source connected to this pin can temporary or permanently control the effective switching duty-cycle. This pin can be used as a voltage mode control input. By connecting pin 11 to Ground, the MC44603 can be shut down.
12	R_P STAND-BY	A voltage level applied to the R_P STAND-BY pin determines the output power level at which the oscillator will turn into the reduced frequency mode of operation (i.e. standby mode). An internal hysteresis comparator allows to return in the normal mode at an higher output power level.
13	E/A OUT	The error amplifier output is made available for loop compensation.
14	VOLTAGE FEEDBACK	This is the inverting input of the Error Amplifier. It can be connected to the switching power supply output through an optical (or else) feedback loop or to the subdivided V_{cc} voltage in case of primary sensing technic.
15	R_F STAND-BY	The reduced frequency or stand-by frequency programming is made by the R_F STAND-BY resistance choice.
16	R_{REF}	The R_{REF} values fixes the internal reference current which is used to perform the precise oscillator waveform. The current range goes form 100μA to 500μA. The input pin R_P STAND-BY ,R_F STAND-BY and SOFT START are receiving a portion of that reference current allowing to build on those pins a reference voltage level with just a resistor.

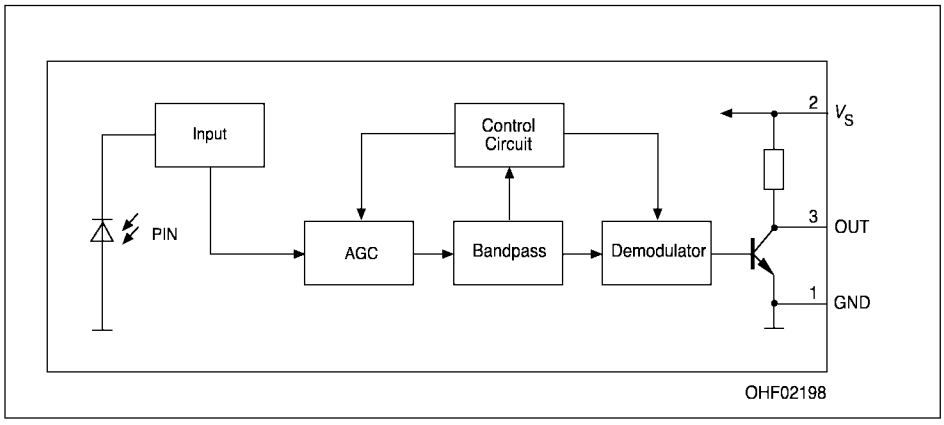
SFH 506

IR-RECEIVER / DEMODULATOR DEVICE

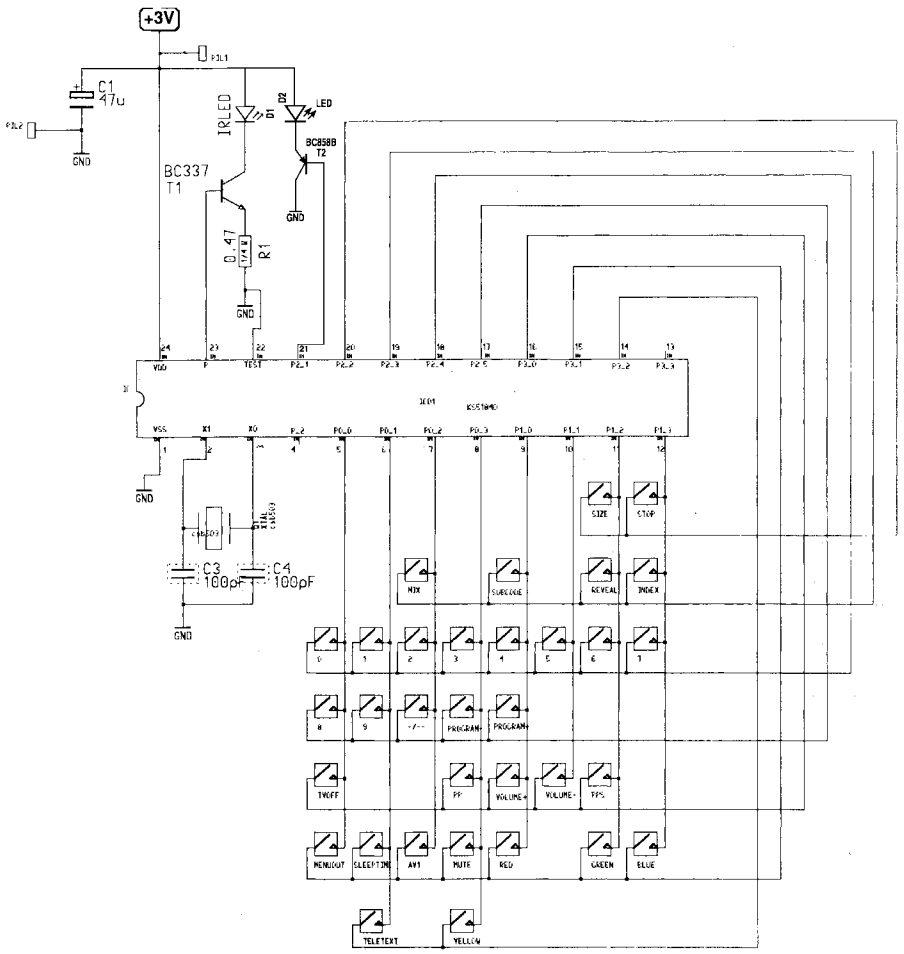
FEATURES

- Photodiode with hybride integrated circuit
- Available for several Carrier frequencies
- Black epoxy resin , daylight filter optimized for 950 nm
- High immunity against ambient light
- Low power consumption
- 5 V supply voltage
- High sensitivity (internal shield case)
- TTL and CMOS compatibility
- Continuous transmission possible (t_{pi} / $T \leq$ 0.4)

Block Diagram



REMOTE CONTROL CIRCUIT DIAGRAM



STV8223B

MULTISTANDARD VIDEO AND SOUND IF SYSTEM WITH AUDIO AND VIDEO SWITCHES

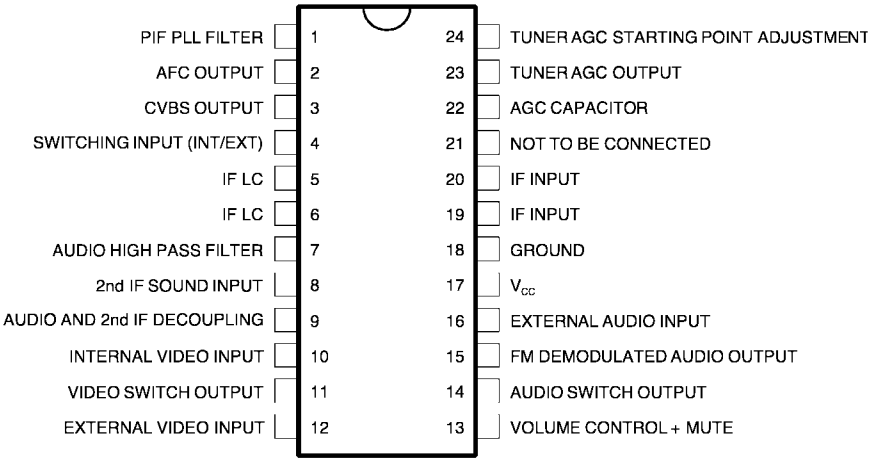
DESCRIPTION

The STV8223B is a picture and sound IF processor for multistandard application with very few external components and adjustments.

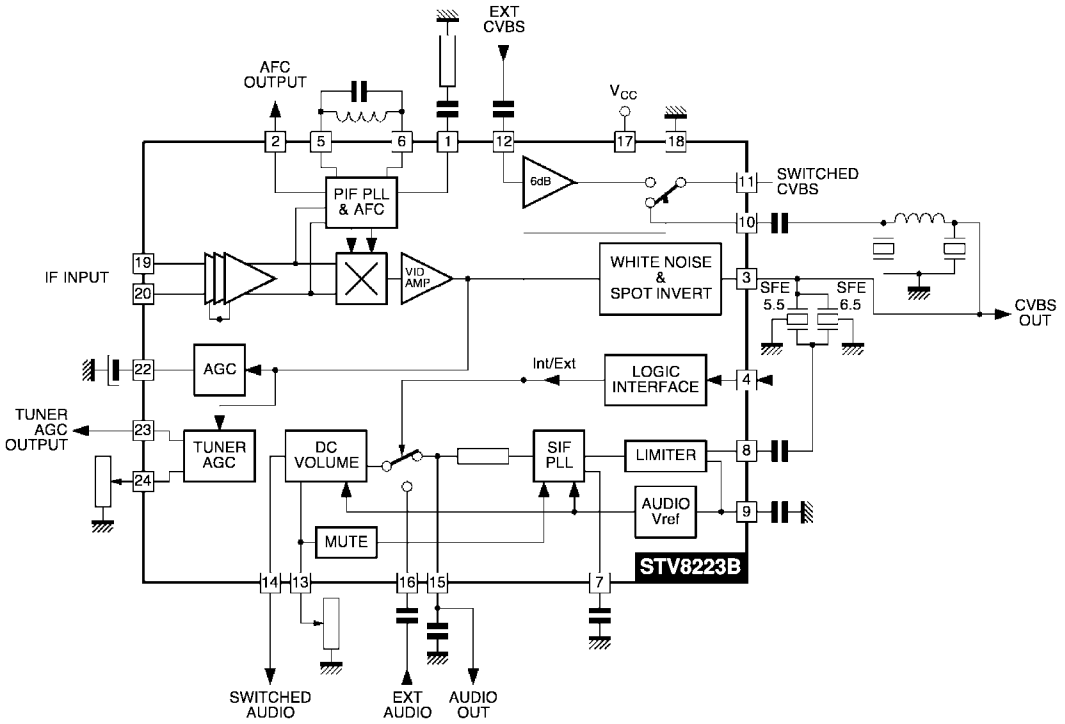
It provides the audio and video switches for one SCART plug application.

- VIDEO PLL DEMODULATION
- SOUND PLL DEMODULATION
- NEGATIVE MODULATION
- AGC FOR NEGATIVE MODULATION
- AUDIO SWITCH
- DC VOLUME CONTROL
- VIDEO SWITCH

PIN CONNECTIONS



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C, V_{CC} = 9V, IF input = 10mV$_{RMS}$ sync level at B/G,
Video modulation DSB, D = 90% at B/G, f_{PC} = 38.9MHz, f_{SC} = 33.4MHz,
Video BW = 5MHz, Sound carrier input : 5.5MHz, 10mV$_{RMS}$, f_M = 1kHz, Audio BW = 20kHz, Δf = ±50kHz,
Volume attenuation = 0dB, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY						
V_{CC}	Supply Voltage		8	9	12.6	V
I_{CC}	Supply Current	I_{17}, V_{CC} = 9V		70	95	mA
IF AMPLIFIER						
V_{19-20}	Input Sensitivity (RMS)	-3dB Video at Output		70		µV$_{RMS}$
R_{19-20}	Differential Input Resistance			2		kΩ
C_{19-20}	Differential Input Capacitance			2		pF
Gr	Gain Control Range			68		dB
	Max Input Signal	+1dB Video at Output		180		mV$_{RMS}$
SYNCHRONOUS VIDEO DEMODULATOR						
DF_{PC}	Vision Carrier Capture		-1.4		1.6	MHz
AFC						
S2	AFC Slope	See Figure 21		0.2		µA/kHz
DEMODULATED VIDEO OUTPUT (Pin 3)						
V_{A3}	Amplitude	Top Sync to White	2	2.3	2.6	V_{PP}
BG vs L	Amplitude Difference				10	%
V_{S3}	Top Sync Level	B/G	1.6	1.9	2.2	V
	Zero Carrier Level	B/G		4.4		V
BW	Bandwidth	-3dB Video Signal	7	9		MHz
Dg	Differential Gain			6	8	%
Dp	Differential Phase			3	6	Degree
Vr3c	Residual Carrier Signal (RMS Value)			1	10	mV
Vr3h	Residual 2nd Harmonic (RMS Value)			1	10	mV
I_3	Internal Bias of Emitter Follower		3	5		mA
S/N	Signal to Noise Ratio	Note 1 - Weighted CCIR-567	56	61		dB
	Intermodulation 1.07MHz	Note 2		52		dB
V_{WTH}	White Noise Threshold Voltage			4.85		V
V_{WIL}	White Noise Insertion Level			3.6		V
V_{BTH}	Black Noise Threshold Voltage			1.3		V
V_{BIL}	Black Noise Insertion Level			2.5		V
AGC CIRCUIT						
I_{22CBG}	Charging Current		550	950	1300	µA
I_{22DBG}	Discharge Current		12	20	28	µA
C/D	Charging/Discharging Ratio			45		
TUNER AGC						
I_{23}	Maximum Sinked Current		1.5	2	2.5	mA
S23	Current Slope	R_{24} = 5kΩ	100	170	230	µA/dB
I_{23+}	Maximum Tuner Plus Sinked Current	Note 3		40		mA

Notes : 1. $\frac{S}{N} = 20 \log 10 \frac{V_{out\ black\ white}}{V_N\ (mV_{RMS})}$ at BW = 5MHz

2. Video carrier relative level = 0dB, Chroma subcarrier level = -3.2dB, Sound carrier relative level = -20dB. AGC voltage (Pin 22) is adjusted to get 1V_{PP} signal on output (Pin 3).

3. Additional sinked current for large increasing steps of input signal when :
   - Voltage Pin 22 > starting point defined Pin 24.
   - Output signal (Pin 3) saturated (V_3 < V BTH in BG mode).

ELECTRICAL CHARACTERISTICS (continued)
(T_{amb} = 25°C, V_{CC} = 9V, IF input = 10mV_{RMS} sync level at B/G,
Video modulation DSB, D = 90% at B/G, f_{PC} = 38.9MHz, f_{SC} = 33.4MHz,
Video BW = 5MHz, Sound carrier input : 5.5MHz, 10mV_{RMS}, f_M = 1kHz, Audio BW = 20kHz, Δf = ±50kHz,
Volume attenuation = 0dB, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
FM SOUND DEMODULATION						
V_{8S}	Input Sensitivity			150		μV_{RMS}
R_8	Limiter Input Resistance			600		Ω
	DC Voltage (Pin 8)			4.2		V
AMR	Amplitude Modulation Rejection	Note 4	50	61		dB
SVR	Supply Voltage Rejection Ratio	Ripple signal : 100Hz, 0.5V_{PP}	28	33		dB
V_{15}	Detected Audio Output Signal		0.85	1.1	1.4	V_{RMS}
THD	Total Harmonic Distortion			0.2	1	%
R_{15}	Internal Deemphasis Resistor		600	750	900	Ω
S/N	Signal to Noise Ratio	See Note 5, Weighted CCIR 468-4, (quasi peak level) input Pin 8	55	60		dB
	Black Picture (sync only)	Measurement between IF input (Pins 19-20) and audio output (Pin 15) SAW : K2955 BPF : SFE5.5MB	47	52		dB
	White Picture		46	50		dB
	250kHz Square Wave		47	52		dB
VOLUME CONTROL						
V_C Range	Control Range	See Figure 22	72	77		dB
AUDIO SWITCH						
R_{16}	Input Resistance		55	70	85	kΩ
CRtk	Crosstalk		70	80		dB
En	Output Noise Level (Pin 14)	Weighted CCIR 468-4, V_{13} = 0.5V (quasi peak level)		70		μV
EXTHD	THD on External Signal (Pin 14)	V_{IN} = 2V_{RMS}, Attenuation = 0dB		0.1	0.3	%
	Audio Reference Voltage (Pin 9)			4.5		V
VIDEO SWITCH						
V_{DC12}	DC Input Level	No signal	1.6	1.9	2.2	V
V_{S12}	Top Sync. Clamp Level			1.8		V
V_{11}	DC Output Level	No signal	1.7	2	2.3	V
V_{S11}	Top Sync. Clamp Level			1.5		V
	Crosstalk			55		dB
GEX	Gain from Ext. Input to Output		5.5	6	6.5	dB
	Output Swing		4	5		V
I_{12}	Input Current	V_{12} = V_{DC12} = 1.5V		1	5	μA
VBW	Bandwidth	V_{IN} = 1V_{PP}		15		MHz
G_{IN}	Gain from Int. Input to Output		-0.5	0	+0.5	dB
MUTE (Pin 13)						
V_{TH13}	Threshold Voltage Pin 13		0.2	0.3	0.4	V
CONTROL INPUT						
	Negative Modulation	Video : External - Audio : External	7.2			V
	Negative Modulation	Video : Internal - Audio : Internal			1.8	V

Notes : 4. AMR = 20 log $\frac{V_{15}(mV_{RMS})}{V_{AM}}$ (dB) where V_{AM} = output amplitude in AM for f_M = 1kHz and m = 30%

5. $\frac{S}{N}$ = 20 log $\frac{V_{15}(mV_{RMS})}{V_N(mV_{RMS})}$ (dB)

ST6387

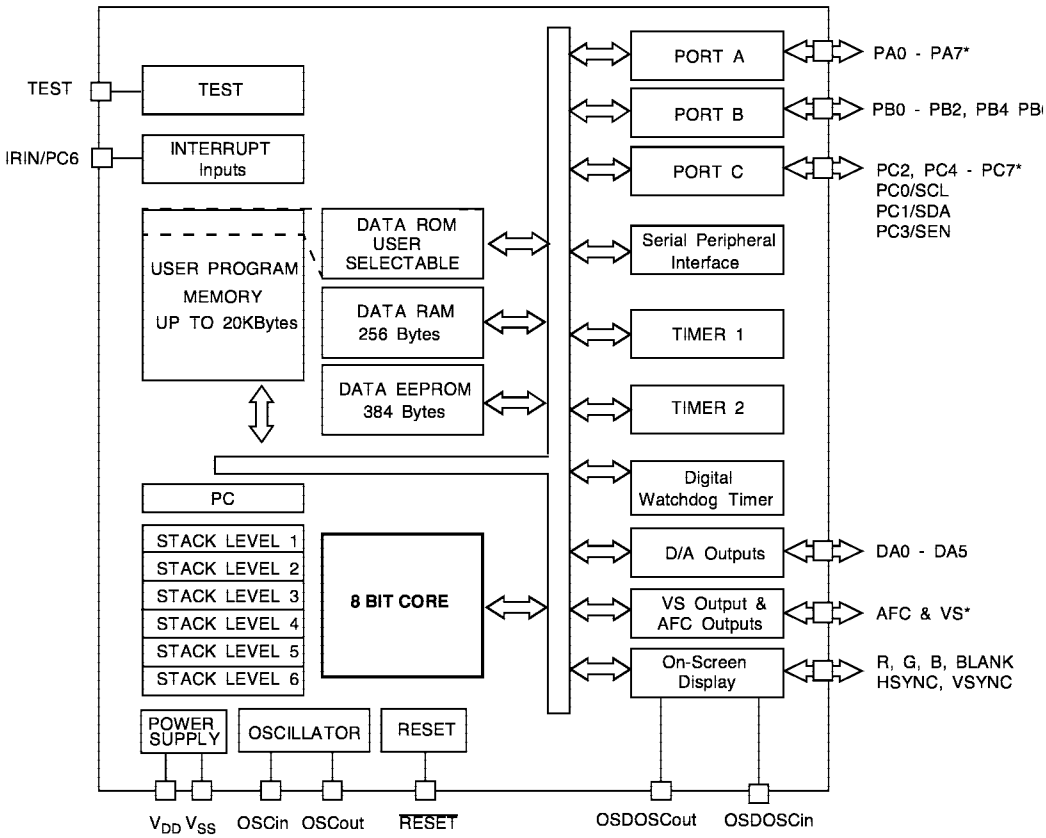
8-BIT MICROCONTROLLER WITH ON-SCREEN-DISPLAY FOR TV TUNING

- 4.5 to 6V supply operating range
- 8MHz Maximum Clock Frequency
- User Program ROM: up to 20140 bytes
- Reserved Test ROM: up to 340 bytes
- Data ROM: user selectable size
- Data RAM: 256 bytes
- Data EEPROM: 384 bytes
- 42-Pin Shrink Dual in Line Plastic Package
- Up to 22 software programmable general purpose Inputs/Outputs, including 2 direct LED driving Outputs
- Two Timers each including an 8-bit counter with a 7-bit programmable prescaler
- Digital Watchdog Function
- Serial Peripheral Interface (SPI) supporting S-BUS/ I 2 C BUS and standard serial protocols
- SPI for external frequency synthesis tuning
- 14 bit counter for voltage synthesis tuning
- Up to Six 6-Bit PWM D/A Converters
- AFC A/D converter with 0.5V resolution
- Five interrupt vectors (IRIN/NMI, Timer 1 & 2, VSYNC, PWR INT.)
- On-chip clock oscillator
- 5 Lines by 15 Characters On-Screen Display Generator with 128 Characters
- All ROM types are supported by pin-to-pin EPROM and OTP versions.

Device Summary

Device	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	AFC	VS	D/A	Colour Pins	EPROM Devices
ST6387	20K	256	384	Yes	Yes	6	3	ST63E87

Block Diagram



PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCin, OSCout. These pins are internally connected to the on-chip oscillator circuit. A quartz crystal or a ceramic resonator can be connected between these two pins in order to allow the correct operation of the MCU with various stability/ cost trade-offs. The OSCin pin is the input pin, the OSCout pin is the output pin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to start the microcontroller to the beginning of its program. Additionally the quartz crystal oscillator will be disabled when the $\overline{\text{RESET}}$ pin is low to reduce power consumption during reset phase.

TEST. The TEST pin must be held at V_{SS} for normal operation.

PA0-PA7. These 8 lines are organized as one I/O port (A). Each line may be configured as either an input with or without pull-up resistor or as an output under software control of the data direction register. Pins PA4 to PA7 are configured as open-drain outputs (12V drive). On PA4-PA7 pins the input pull-up option is not available while PA6 and PA7 have additional current driving capability (25mA, V_{OL}:1V). PA0 to PA3 pins are configured as push-pull.

PB0-PB2, PB4-PB6. These 6 lines are organized as one I/O port (B). Each line may be configured as either an input with or without internal pull-up resistor or as an output under software control of the data direction register.

PC0-PC7. These 8 lines are organized as one I/O port (C). Each line may be configured as either an input with or without internal pull-up resistor or as an output under software control of the data direction register. Pins PC0 to PC3 are configured open-drain (5V drive) in output mode while PC4 PC7 are open-drain with 12V drive and the inp pull-up options does not exist on these four pir PC0, PC1 and PC3 lines when in output mode ε "ANDed" with the SPI control signals and are open-drain. PC0 is connected to the SPI clock si nal (SCL), PC1 with the SPI data signal (SD while PC3 is connected with SPI enable sign (SEN, used in S-BUS protocol). Pin PC4 and P(can also be inputs to software programmable edç sensitive latches which can generate interrupts PC4 can be connected to Power Interrupt whi PC6 can be connected to the IRIN/NMI interru line.

DA0-DA5. These pins are the six PWM D/A outputs of the 6-bit on-chip D/A converters. These lines have open-drain outputs with 12V drive. The output repetition rate is 31.25KHz (with 8MHz clock).

AFC. This is the input of the on-chip 10 levels comparator that can be used to implement the AFC function. This pin is an high impedance input able to withstand signals with a peak amplitude up to 12V.

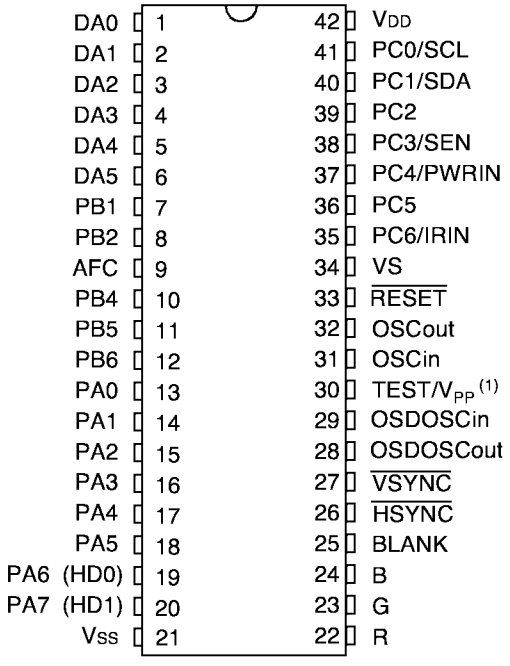
OSDOSCin, OSDOSCout. These are the On Screen Display oscillator terminals. An oscillation capacitor and coil network have to be connected to provide the right signal to the OSD.

HSYNC, VSYNC. These are the horizontal and vertical synchronization pins. The active polarity of these pins to the OSD macrocell can be selected by the user as ROM mask option. If the device is specified to have negative logic inputs, then these signals are low the OSD oscillator stops. If the device is specified to have positive logic inputs, then when these signals are high the OSD oscillator stops. VSYNC is also connected to the VSYNC interrupt.

R, G, B, BLANK. Outputs from the OSD. R, G and B are the color outputs while BLANK is the blanking output. All outputs are push-pull. The active polarity of these pins can be selected by the user as ROM mask option.

VS. This is the output pin of the on-chip 14-bit voltage synthesis tuning cell (VS). The tuning signal present at this pin gives an approximate resolution of 40KHz per step over the UHF band. This line is a push-pull output with standard drive.

Pin configuration



(1) This pin is also the V_{PP} input for OTP/EPROM devices

Pin Summary

Pin Function	Description
DA0 to DA5	Output, Open- Drain, 12V
AFC	Input, High Impedance, 12V
VS	Output, Push- Pull
R, G, B, BLANK	Output, Push- Pull
HSYNC, VSYNC	Input, Pull- up, Schmitt Trigger
OSDOSCin	Input, High Impedance
OSDOSCout	Output, Push- Pull
TEST	Input, Pull- Down
OSCin	Input, Resistive Bias, Schmitt Trigger to Reset Logic Only
OSCout	Output, Push- Pull
RESET	Input, Pull- up, Schmitt Trigger Input
PA0- PA3	I/ O, Push- Pull, Software Input Pull- up, Schmitt Trigger Input
PA4- PA5	I/ O, Open- Drain, 12V, No Input Pull- up, Schmitt Trigger Input
PA6- PA7	I/ O, Open- Drain, 12V, No Input Pull- up, Schmitt Trigger Input, High Drive
PB0- PB2	I/ O, Push- Pull, Software Input Pull- up, Schmitt Trigger Input
PB4- PB6	I/ O, Push- Pull, Software Input Pull- up, Schmitt Trigger Input
PC0- PC3	I/ O, Open- Drain, 5V, Software Input Pull- up, Schmitt Trigger Input
PC4- PC7	I/ O, Open- Drain, 12V, No Input Pull- up, Schmitt Trigger Input
V_{DD}, V_{SS}	Power Supply Pins

DC ELECTRICAL CHARACTERISTICS

(TA = 0 to +70°C unless otherwise specified).

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage	All I/O Pins			0.2xV$_{DD}$	V
V_{IH}	Input High Level Voltage	All I/O Pins	0.8xV$_{DD}$			V
V_{HYS}	Hysteresis Voltage(1)	All I/O Pins V_{DD} = 5V		1.0		V
V_{OL}	Low Level Output Voltage	DA0-DA5, PB0-PB6, OSD Outputs, PC0-PC7, O0, O1, PA0-PA5 V_{DD} = 4.5V I_{OL} = 1.6mA I_{OL} = 5.0mA			 0.4 1.0	 V V
V_{OL}	Low Level Output Voltage	PA6-PA7 V_{DD} = 4.5V I_{OL}= 1.6mA I_{OL}= 25mA			 0.4 1.0	 V V
V_{OL}	Low Level Output Voltage	OSDOSCout OSCout V_{DD} = 4.5V I_{OL}= 0.4mA			0.4	V
V_{OL}	Low Level Output Voltage	VS Output V_{DD} = 4.5V I_{OL}= 0.5mA I_{OL}= 1.6mA			 0.4 1.0	 V V
V_{OH}	High Level Output Voltage	PB0-PB7, PA0-PA3, OSD Outputs V_{DD} = 4.5V I_{OH} = − 1.6mA	4.1			V
V_{OH}	High Level Output Voltage	OSDOSCout, OSCout, V_{DD} = 4.5V I_{OH}= − 0.4mA	4.1			V
V_{OH}	High Level Output Voltage	VS Output V_{DD} = 4.5V I_{OH}= - 0.5mA	4.1			V
I_{PU}	Input Pull Up Current Input Mode with Pull-up	PB0-PB6, PA0-PA3, PC0-PC3, V_{IN}= V_{SS}	− 100	− 50	− 25	μA
I_{PU}	Input Pull Up Current	OSCin V_{IN}= V_{SS}	− 50	− 25	− 10	μA
I_{IL} I_{IH}	Input Leakage Current	OSCin V_{IN}= V_{SS} V_{IN}= V_{DD}	− 10 0.1	− 1 1	− 0.1 10	μA
I_{IL}	Input Pull-down current in RESET	OSCin	100			μA
I_{IL} I_{IH}	Input Leakage Current	All I/O Input Mode no pull-up OSDOSCin V_{IN}= V_{DD} or V_{SS}	-10		10	μA
V_{DD}RAM	RAM Retention Voltage in RESET Mode		1.5			V
I_{IL} I_{IH}	Input Leakage Current	Reset Pin with Pull-up V_{IN}= V_{SS}	− 50	− 30	− 10	μA

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{IL} I_{IH}	Input Leakage Current	AFC Pin V_{IH}= V_{DD} V_{IL}= V_{SS} V_{IH} = 12.0V	-1		1 40	µA
I_{OH}	Output Leakage Current	DA0-DA5, PA4-PA5, PC0-PC7, O0, O1 V_{OH} = V_{DD}			10	µA
I_{OH}	Output Leakage Current High Voltage	DA0-DA5, PA4-PA7, PC4-PC7, O0, O1 V_{OH} = 12V			40	µA
I_{DD}	Supply Current RUN Mode	f_{OSC} = 8MHz, ILoad= 0mA V_{DD}= 6.0V		6	16	mA
I_{DD}	Supply Current WAIT Mode	f_{OSC}= 8MHz, ILoad= 0mA V_{DD}= 6V		3	10	mA
I_{DD}	Supply Current at transition to RESET	f_{OSC}= Not App, ILoad= 0mA V_{DD}= 6V		0.1	1	mA
V_{ON}	Reset Trigger Level ON	RESET Pin			0.3xV_{DD}	V
V_{OFF}	Reset Trigger Level OFF	RESET Pin	0.8xV_{DD}			V
V_{TA}	Input Level Absolute Tolerance	A/D AFC Pin V_{DD}= 5V			± 200	mV
V_{TR}	Input Level Relatice Tolerance(1)	A/D AFC Pin Relative to other levels V_{DD}= 5V			± 100	mV

Note 1. Not 100% Tested

AC ELECTRICAL CHARACTERISTICS

(TA = 0 to +70°C, f_{OSC}=8MHz, V_{DD}=4.5 to 6.0V unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{WRES}	Minimum Pulse Width	RESET Pin	125			ns
t_{OHL}	High to Low Transition Time	PA6, PA7 V_{DD} = 5V, CL = 100pF(2)		100		ns
t_{OHL}	High to Low Transition Time	DA0-DA5, PB0-PB6, OSD Outputs, PC0-PC7 V_{DD} = 5V, CL = 100pF		20		ns
t_{OLH}	Low to High Transition Time	PB0-PB6, PA0-PA3, OSD Outputs, PC0-PC3 V_{DD} = 5V, CL = 100pF		20		ns
f_{DA}	D/A Converter Repetition Frequency (1)			31.25		kHz
f_{SIO}	SIO Baudrate(1)			62.50		kHz
t_{WEE}	EEPROM Write Time	T_A = 25°C One Byte		5	10	ms
Endurance	EEPROM WRITE/ERASE Cycles	Q_A L_{OT} Acceptance Criteria	300,000	> 1 million		cycles
Retention	EEPROM Data Retention(4)	T_A = 25°C	10			years
C_{IN}	Input Capacitance(3)	All Inputs Pins			10	pF
C_{OUT}	Output Capacitance(3)	All Outputs Pins			10	pF
COSCin, COSCout	Oscillator Pins Internal Capacitance (3)			5		pF
COSDin, COSDout	Oscillator Pins External Capacitance (3)	Recommended	15		25	pF

Notes:

1. A clock other than 8MHz will affect the frequency response of those peripherals (D/A, and SPIs) whose clock is derived from the system clock.
2. The rise and fall times of PORT A have been increased in order to avoid current spikes while maintaining a high drive capabi
3. Not 100% Tested
4. Based on extrapolated data

STV2112

BUS CONTROLLED PAL/SECAM TV PROCESSOR

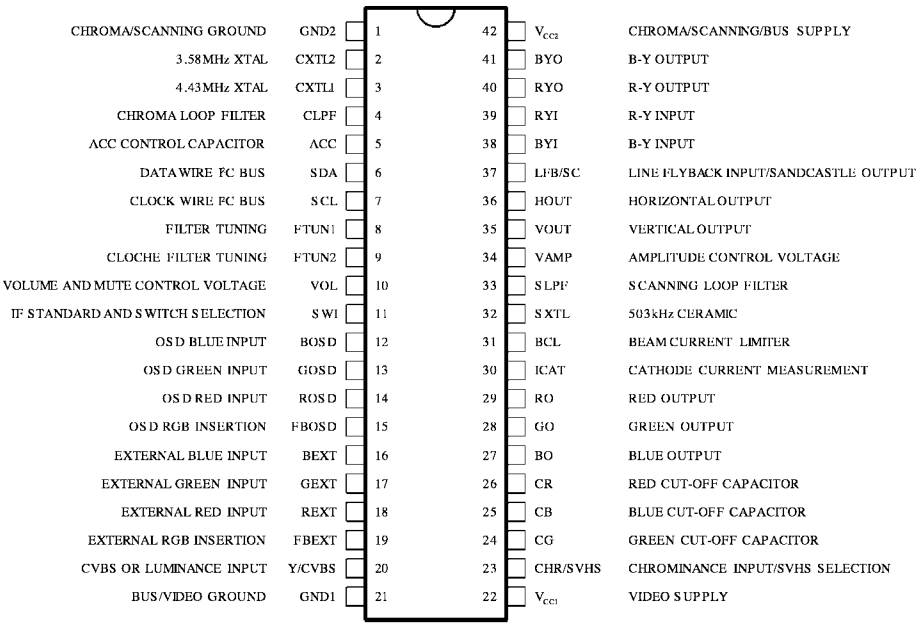
DESCRIPTION

The STV2112 is a fully bus controlled IC for TV luma, chroma and deflection processing.

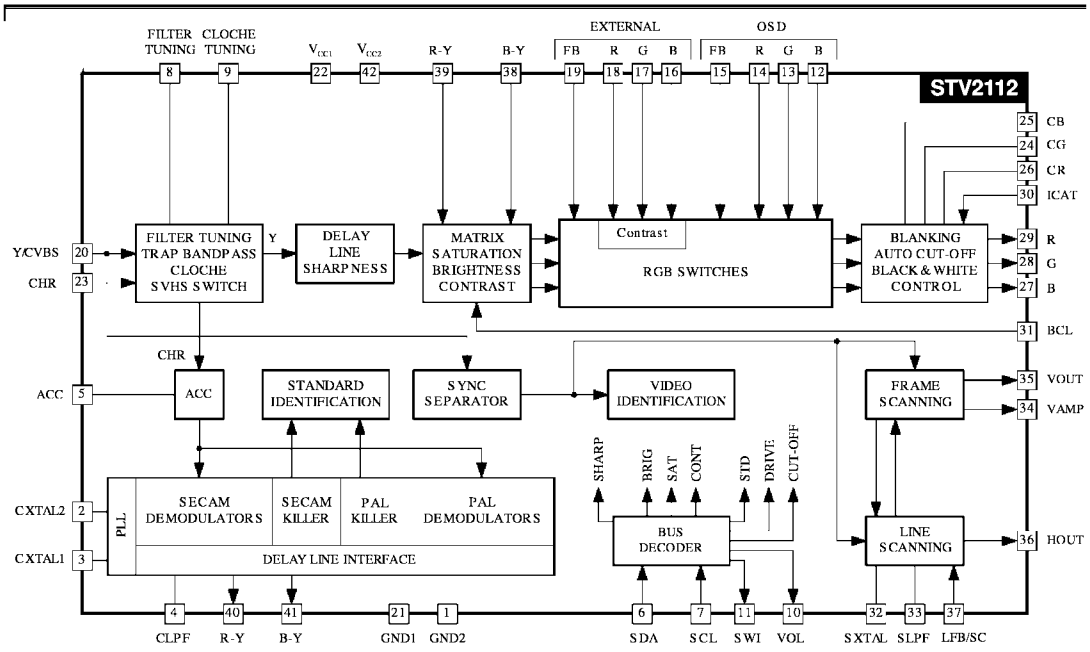
Used with STV8224 (PIF/SIF/switches), TDA1771 or TDA8174 (frame booster), STV2180 (delay line), it allows to design a PAL/SECAM (BGDKIL) set with very few external components and no adjustment.

- I^2C BUS CONTROL OF ALL FUNCTIONS
- INTEGRATED FILTERS (TRAP, BANDPASS, CLOCHE)
- INTEGRATED LUMINANCE DELAY LINE
- PAL/SECAM CHROMA DEMODULATORS
- AUTOMATIC CUT-OFF CURRENT LOOP
- TWO RGB INPUTS
- SVHS SWITCH
- TWO PLLs HORIZONTAL DEFLECTION
- VERTICAL COUNT DOWN
- VERY FEW EXTERNAL COMPONENTS

PIN CONNECTIONS



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

1 - DEFLECTION CIRCUIT

Note : [X,Y] : line number referred to the internal line counter numbering

- Fully integrated synch. separator, with a low pass filter, a black level alignment of the Y/CVBS input, a slicing level at 2/3,1/3 of the sync. pulse amplitude.
- Frame sync. pulse locked on 2 f_H frequency to perfect interlace.
- 500kHz VCO with an external ceramic resonator.
- Two phase locked loops
  ∞the first PLL locks the VCO on the video signal frequency,
  ∞the second PLL compensates the line transistor storage time.
- Three time constants for the first PLL.
  ∞the long time constant is used for normal operation
  ∞the short time constant is automatically used during the frame retrace and in search mode of VCR when the frame pulse is outside [258,264] and [309,314].
  ∞very long time constant when no video recognition

  Time constants in normal operation (automatic selection of time constants) :

  50Hz input signal :
  - short time constant : [306, 21]
  - long time constant : the rest of the field

  ∞inhibition of the first PLL :
  the first locked loop is opened from line 309 to line 4.5 (or 314) in 50Hz mode.
  ∞the time constants values are chosen by means of external components.
  ∞possibility to force the short time constant through the bus.
  ∞possibility to force the very long time constant through the bus.
- Video identification : coincidence detector between the line synchro top and a line frequency window from the first PLL. The video identification status is available in the output register of the I^2C bus decoder.
- Generation of burst gate pulses and line frequency signals from the first PLL to drive the chroma and video circuits. The burst gate pulse is also sent to the sandcastle generator.
- Frame synchro window :
  [248, 352] catching
- Field frequency selection windows :
  [288, 352] 50Hz mode selection window
- frame blanking pulse :
  from line 0 to 21 in 50Hz mode
- Vertical output pulse is 10.5 lines long.
- Horizontal output pulse : 28µs line pulse on an open collector output;
- Start up circuit : the horizontal output is at a high level when V_{CC} increases from 0 to 6.8V. On shutting down, horizontal pulses are disabled when V_{CC} is below 6.2V.
- Soft-start circuit : the duty cycle of the horizontal output is 78 % (Thigh/(Thigh + TLow)) when V_{CC1} is lower than (0.75 x V_{CC2}), during the rising time.
  During the falling time, a 78% duty cycle HOUT pulse is provided when V_{CC1} is lower than (0.60 x V_{CC2}).
- Possibility to disable the horizontal output pulse through the bus (force a high level on HOUT).
- Horizontal position adjustment controlled by bus.
- Bus controlled output voltage to adjust the vertical amplitude; this voltage permits to adjust the slope of the vertical sawtooth generated by the external frame booster.
- Bus controlled vertical position ; the high level of the vertical pulse permits to adjust the vertical position.
- Bus controlled 4/3-16/9 selection : the low level of the vertical pulse is 0.1V when 16/9 is selected, 2V when 4/3 is selected.
- Combined flyback input and sandcastle output (Pin 37).
  Two thresholds on LFB/SCO Pin : The lowest threshold (0.7V) permits to extract the line blanking pulse; the highest threshold (2V) permits to extract the line pulse for PLL2.
  The sandcastle signal at Pin 37 is used to control the external baseband chroma delay line.

FUNCTIONAL DESCRIPTION (continued)

2 - FILTERS

- Integrated trap filter :

$$Q = \frac{1}{\frac{f_o}{f_{-3dB}} - \frac{f_{-3dB}}{f_o}}$$

Q = 1.7 at sharp. min
Q = 3.0 at sharp. max

Center frequency : - 4.43MHz for PAL
- 4.25MHz, for SECAM (f_{-3dB} = 3MHz ; -20dB rejection between 4.1MHz and 4.4MHz)

- Integrated chroma bandpass :
  Q = 3.5
  Center frequency : 4.43MHz, 3.58MHz
- Integrated cloche filter for SECAM :
  Q = 16
  Center frequency : 4.286MHz
- Integrated delay line :
  Bandwidth = 8MHz
- Integrated low pass filter for deflection part.
- All filters are tuned with a reference phase locked loop. 3/25
  The PLL consists of a lowpass filter, a phase comparator, a loop filter (with an external capacitor). The reference signal is the continuous carrier wave from the VCO (4.43MHz).
  The PLL adjusts the center frequency of the lowpass so that it is equal to the reference signal. The tuning voltage of the PLL is used to adjust all other filters.
  The cloche filter is fine tuned with a second PLL operating during frame retrace.

3 - VIDEO CIRCUIT

- 2 RGB inputs : RGB (OSD) input has priority against the RGBext. Maximum contrast on RGB (OSD). -10dB range contrast control on RGBext. Possibility to disable the RGBext insertion through the bus.
- Oversize blanking capability on FB(OSD)(Pin15) input. The RGB ouputs will be blanked when the voltage on Pin 15 will exceed the second threshold at 1.9V (blanking threshold) : the whole field is blanked but not the inserted cut-off pulses. The OSD insertion threshold is 0.7V.
- Automatic cut-off current loop : 2V cut-off range. Sequential cut-off current measurement during the three lines after the frame blanking signal. Leakage current measurement during the frame blanking, memorization on an internal capacitor.
- Warm up detector.
- Beam current limiter DC voltage input.
  The beam current limiter control voltage will act on contrast first, then the brightness will be decreased when contrast attenuation reaches -5dB.
- Bus control of the red, green and blue channel gain (White point adjustment)
- Bus control of the red and green DC levels (black point adjustment)
- PAL and SECAM matrix).
- Switch-off of the trap filter in SVHS mode.
- Bus controlled contrast on luminance (20dB range)
- Bus controlled saturation (50dB range)
- Bus controlled brightness : 40% range at maximum contrast.
- Bus controlled sharpness (peaking) ; sharpness active in PAL standard only.
- Noise coring function on sharpness.

FUNCTIONAL DESCRIPTION (continued)

4 - CHROMA CIRCUIT

4.1 - PAL/SECAM Decoders

- SVHS inputs ; bus controlled SVHS mode.
- 30dB range ACC
- Use of an external base band delay line (STV2180 recommended)
- Automatic standard identification, with possibility to force the standard through the bus.

4.2 - PAL Decoder

- ACC done by peak detector on synchronous demodulation of the burst
- Fully integrated killer functions.
- VCO using two standard crystals : 4.43MHz and 3.58MHz.
  3.58MHz crystal is temporarily requested on this version to achieve proper standard identification.

  XTAL SPECIFICATION :
  Frequency :
  4.433619MHz (PAL/SECAM)

  Vibration mode : Fondamental, series resonance (no serial capacitor)
  Motional capacity : 13fF ±3fF
  Resonance resistance : < 70Ω
  Shunt capacitance : < 7pF
  Spurious response : No resonance at $3*f_o$ ±3kHz
- 0^o and $\pm 90^o$ demodulation angles for PAL

4.3 - SECAM Decoder

- ACC
- Fully integrated killer
- Two integrated discriminators with two PLL
- Integrated deemphasis

4.4 - Standard Identification

- Sequential identification.
- 3 identification sequences : XTAL1 (4.43MHz) mode to identify PAL, XTAL2 (3.58MHz) mode not used, SECAM mode (XTAL1 selection).
- PAL priority
- the SECAM mode is locked after two identified SECAM sequences
- the SECAM mode can be selected in 50Hz only
- Blanking of the (R-Y) and B-Y) outputs during color search mode.

5 - OTHER FUNCTIONS : IF CONTROLS

5.1 - Volume Control and Mute

The volume control voltage range on Pin 10 is from 0.5V to 5V. A low voltage on Pin 10 (below 0.2V) will mute the FM demodulator of the IF circuit STV8224. It will put the volume at the minimum level and thus there will be no sound either in TV mode or SCART mode.

The volume control voltage and the mute level are controlled by the bus.

5.2 - IF Standard and TV/SCART Mode Selection

The selection of IF standard (positive or negative vision modulation) and the TV/SCART mode is controlled by the bus. The selection is converted in four voltages on Pin 21.
The lowest voltage selects the TV mode and the NEGATIVE vision modulation.
The highest voltage (open collector output with internal pull-up resistor to V_{CC}) selects the SCART mode and the NEGATIVE vision modulation.
The two other intermediate voltages select either TV mode and POSITIVE vision modulation or SCART mode and POSITIVE vision modulation.

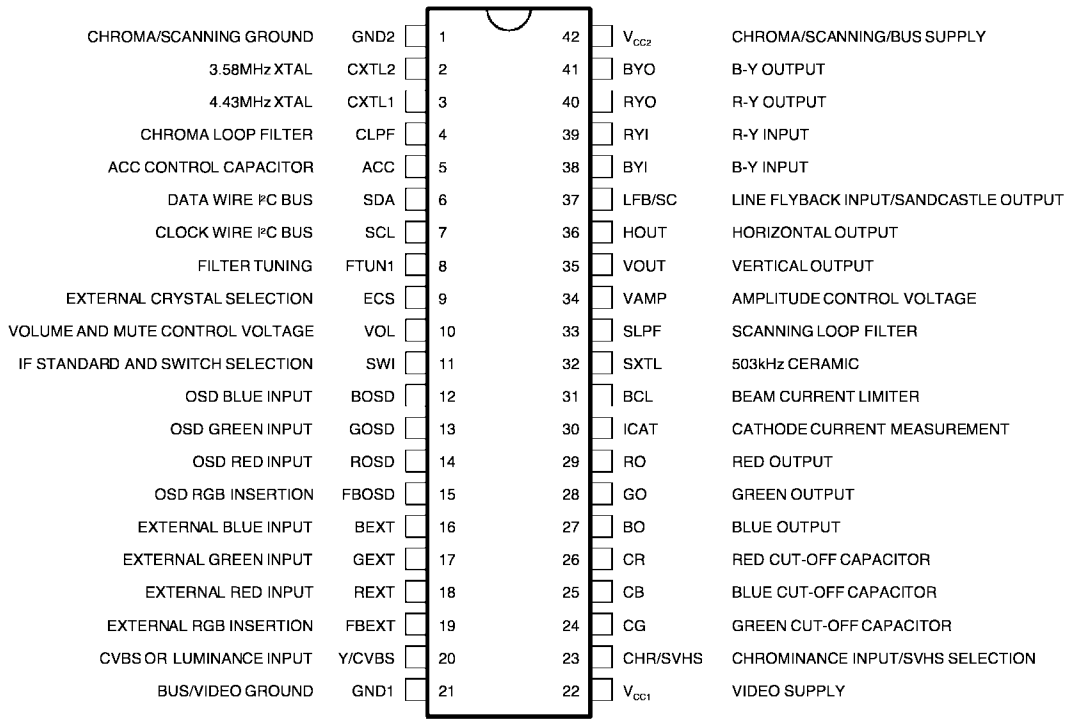
STV2116A

BUS CONTROLLED PAL TV PROCESSOR

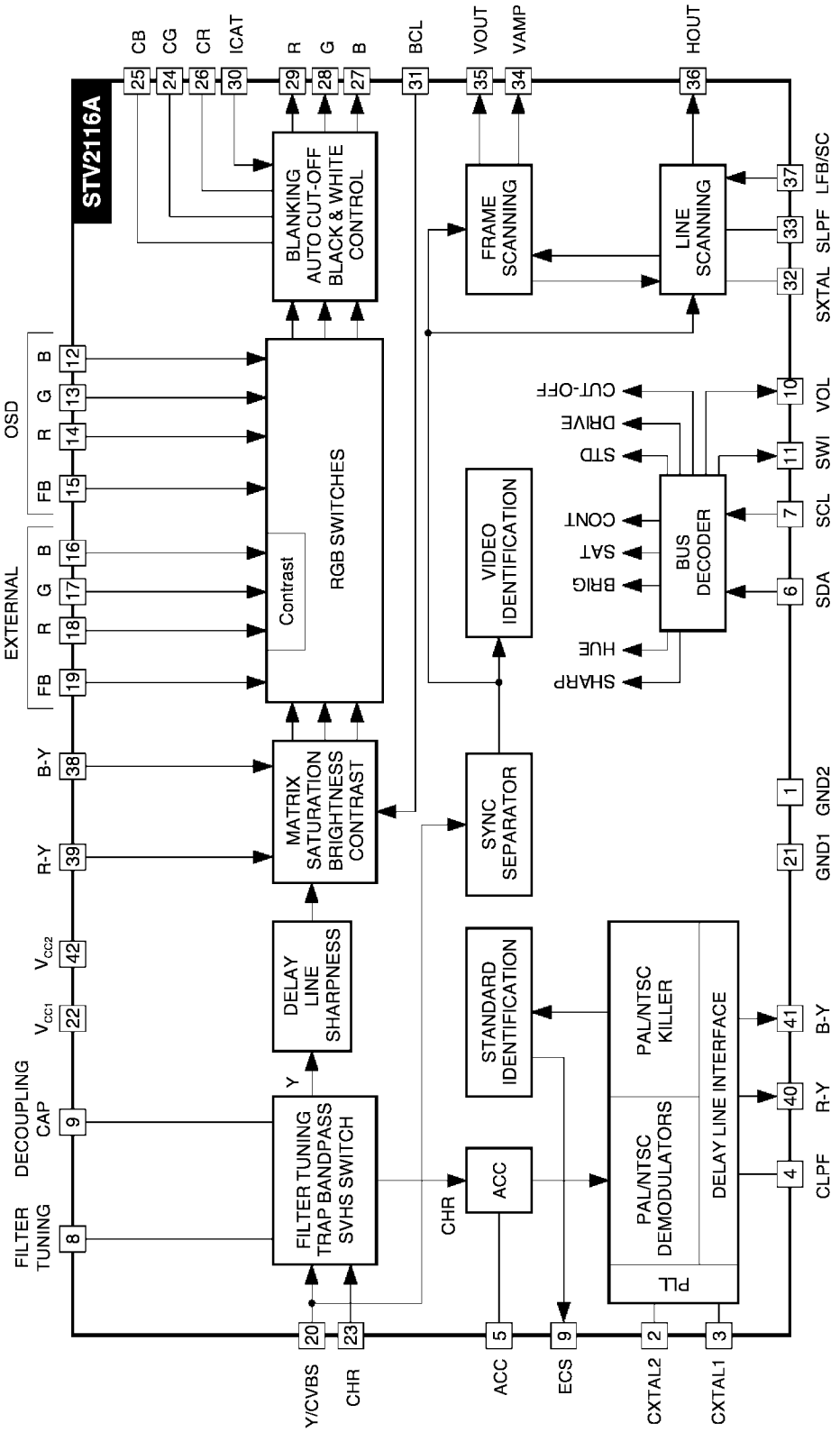
The STV2116A is a fully bus controlled IC for TV luma, chroma and deflection processing.

- I^2C BUS CONTROL OF ALL FUNCTIONS
- INTEGRATED FILTERS (TRAP, BANDPASS)
- INTEGRATED LUMINANCE DELAY LINE
- PAL/NTSC CHROMA DEMODULATORS
- NTSC AUTOMATIC FLESH TONE CONTROL
- AUTOMATIC CUT-OFF CURRENT LOOP
- TWO RGB INPUTS
- SVHS SWITCH
- TWO PLLs HORIZONTAL DEFLECTION
- VERTICAL COUNT DOWN
- 3 CRYSTALS APPLICATION CAPABILITY
- BLUE SCREEN
- VERY FEW EXTERNAL COMPONENTS

PIN CONNECTIONS



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

1 - DEFLECTION CIRCUIT

Note : [X,Y] : line number referred to the internal line counter numbering

- Fully integrated synch. separator, with a low pass filter, a black level alignment of the Y/CVBS input, a slicing level at 2/3,1/3 of the sync. pulse amplitude.
- Frame sync. pulse locked on 2 f_H frequency to perfect interlace.
- 500kHz VCO with an external ceramic resonator.
- Two phase locked loops
  - ∝the first PLL locks the VCO on the video signal frequency,
  - ∝the second PLL compensates the line transistor storage time.
- Three time constants for the first PLL.
  - ∝the long time constant is used for normal operation
  - ∝the short time constant is automatically used during the frame retrace and in search mode of VCR when the frame pulse is outside [258,264] and [309,314].
  - ∝very long time constant when no video recognition

  Time constants in normal operation (automatic selection of time constants) :

  50Hz input signal :
  - short time constant : [306, 21]
  - long time constant : the rest of the field

  60Hz input signal :
  - short time constant : [0, 16]
  - long time constant : the rest of the field

  - ∝inhibition of the first PLL : the first locked loop is opened from line 309 to line 4.5 (or 314) in 50Hz mode. It is opened from line 258 to line 5.5 (or 264) in 60Hz mode.
  - ∝the time constants values are chosen by means of external components.
  - ∝possibility to force the short time constant through the bus.
  - ∝possibility to force the very long time constant through the bus.
- Video identification : coincidence detector between the line synchro top and a line frequency window from the first PLL. The video identification status is available in the output register of the I^2C bus decoder.
- Generation of burst gate pulses and line frequency signals from the first PLL to drive the chroma and video circuits. The burst gate pulse is also sent to the sandcastle generator.
- Frame synchro window : [248, 352] catching
- Field frequency selection windows :

  [248, 288] 60Hz mode selection if two consecutive frame pulses occur inside this window, otherwise 50Hz mode selection.

  [288, 352] 50Hz mode selection window
- frame blanking pulse :
  from line 0 to 21 in 50Hz mode
  from line 0 to 16 in 60Hz mode
- Vertical output pulse is 10.5 lines long.
- Horizontal output pulse : 28µs line pulse on an open collector output;
- Start up circuit : the horizontal output is at a high level when V_{CC} increases from 0 to 6.8V. On shutting down, horizontal pulses are disabled when V_{CC} is below 6.2V.
- Soft-start circuit : the duty cycle of the horizontal output is 78 % (Thigh/(Thigh + TLow)) when V_{CC1} is lower than (0.75 x V_{CC2}), during the rising time. During the falling time, a 78% duty cycle HOUT pulse is provided when V_{CC1} is lower than (0.60 x V_{CC2}).
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- Combined flyback input and sandcastle output (Pin 37). Two thresholds on LFB/SCO Pin : The lowest threshold (0.7V) permits to extract the line blanking pulse; the highest threshold (2V) permits to extract the line pulse for PLL2. The sandcastle signal at Pin 37 is used to control the external baseband chroma delay line.

2 - FILTERS

- Integrated trap filter :

$$Q = \frac{1}{\frac{f_o}{f_{-3dB}} - \frac{f_{-3dB}}{f_o}}$$

Q = 1.7 at sharp. min
Q = 3.0 at sharp. max

Center frequency : - 4.43MHz,
3.58MHz for PAL, NTSC

- Integrated chroma bandpass : Q = 3.5
  Center frequency : 4.43MHz, 3.58MHz
- Integrated delay line : Bandwidth = 8MHz
- Integrated low pass filter for deflection part.
- All filters are tuned with a reference phase locked loop. The PLL consists of a lowpass filter, a phase comparator, a loop filter (an external capacitor). The reference signal is the continuous carrier wave from the VCO (4.43MHz or 3.58MHz). The PLL adjusts the center frequency of the lowpass so that it is equal to the reference signal. The tuning voltage of the PLL is used to adjust all other filters.

FUNCTIONAL DESCRIPTION (continued)

3 - VIDEO CIRCUIT

- 2 RGB inputs : RGB (OSD) input has priority against the RGBext. Maximum contrast on RGB (OSD). -10dB range contrast control on RGBext. Possibility to disable the RGBext insertion through the bus.
- Oversize blanking capability on FB(OSD)(Pin15) input. The RGB ouputs will be blanked when the voltage on Pin 15 will exceed the second threshold at 1.9V (blanking threshold) : the whole field is blanked but not the inserted cut-off pulses. The OSD insertion threshold is 0.7V.
- Automatic cut-off current loop : 2V cut-off range. Sequential cut-off current measurement during the three lines after the frame blanking signal. Leakage current measurement during the frame blanking, memorization on an internal capacitor.
- Possibility to force through the bus the inserted cut-off pulses on lines 23/24/25(CCIR) in 50Hz and 60Hz mode.
- Warm up detector.
- Beam current limiter DC voltage input. The beam current limiter control voltage will act on contrast first, then the brightness will be decreased when contrast attenuation reaches -5dB.
- Bus control of the red, green and blue channel gain (White point adjustment)
- Bus control of the red and green DC levels (black point adjustment)
- PAL matrix, specific NTSC matrix when demodulation angles are (0^o, 104^o).
- Switch-off of the trap filter in SVHS mode.
- Bus controlled contrast on luminance (20dB range)
- Bus controlled saturation (50dB range)
- Bus controlled brightness : 40% range at maximum contrast.
- Bus controlled sharpness (peaking).
- Noise coring function on sharpness.
- Bus controlled blue screen feature

4 - CHROMA CIRCUIT

4.1 - PAL/NTSC Decoders

- SVHS inputs ; bus controlled SVHS mode.
- 30dB range ACC.
- Use of an external base band delay line (STV2180 recommended).
- Automatic standard identification, with possibility to force the standard through the bus.
- ACC done by peak detector on synchronous demodulation of the burst.
- Fully integrated killer functions.
- VCO using two standard crystals : 4.43MHz and 3.58MHz. One crystal is internally selected depending on the standard selection.
- 3 crystals application capability : one crystal on Pin XTAL1 (4.43MHz or 3.58MHz), two crystals on Pin XTAL 2 (3.58MHz only) which can be selected by Pin 9 out signal.
  XTAL SPECIFICATION :
  Frequency : 4.433619MHz (PAL)
  3.579545MHz (NTSC M)
  3.575611MHz (PAL M)
  3.582056MHz (PAL N)
  Vibration mode : Fondamental, series resonance (no serial capacitor)
  Motional capacity : 13fF ±3fF
  Resonance resistance : < 70Ω
  Shunt capacitance : < 7pF
  Spurious response : No resonance at $3*f_o$ ±3kHz
- 0^o and $\pm 90^o$ demodulation angles for PAL
- (0^o, 90^o) or (0^o,104^o) = demodulation angles for NTSC. The selection of 90^o or 104^o is made through the bus.
- Bus control Hue adjustment in NTSC mode.
- NTSC automatic flesh control. Bus controlled disable.
- Switchable chroma demodulator gain (+6dB) for NTSC only application, when no external chroma delay line is used.

4.2 - Standard Identification

- Sequential identification.
- 3 identification sequences : XTAL1 (4.43MHz) mode to identify either PAL or NTSC, XTAL2 (3.58MHz) mode to identify either PAL or NTSC, no SECAM signal checking. In case of single standard operation, we recommend to force this standard by the bus which permits the use of only one crystal.
- Blanking of the (R-Y) and B-Y) outputs during color search mode.

5 - OTHER FUNCTIONS : IF CONTROLS

5.1 - Volume Control and Mute

The volume control voltage range on Pin 10 is from 0.5V to 5V. A low voltage on Pin 10 (below 0.1V) will mute the FM demodulator of the IF circuit (STV8223). Thus there will be no sound either on the speaker or an audio output plug.
The volume control voltage and the mute level are controlled by the bus.

5.2 - TV/SCART Mode Selection

The selection of the TV/External (AV) mode is controlled by the bus. The selection is converted in two voltages on Pin 11.
The lowest voltage selects the TV mode.
The highest voltage (open collector output with internal pull-up resistor to V_{CC}) selects the External (AV) mode.

STV2180A

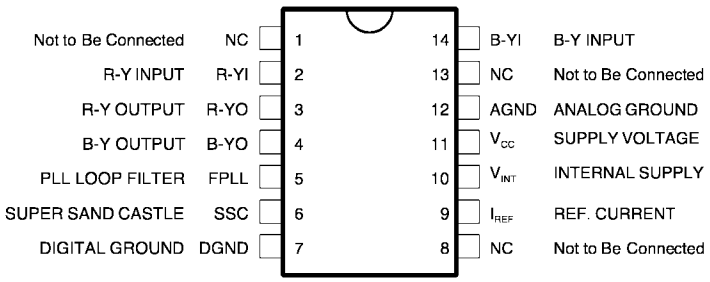
BASE BAND CHROMA DELAY LINE

DESCRIPTION

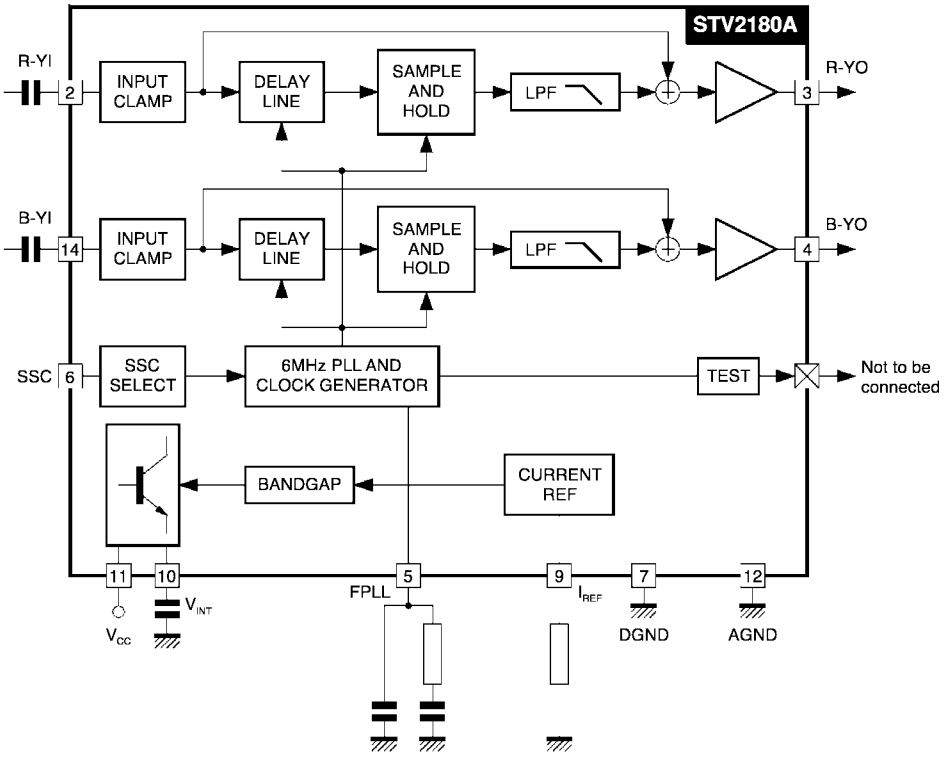
The STV2180A is an integrated base band chroma delay line with one line delay, which has been designed to match chroma decoders with colour difference signal outputs (R-Y) and (B-Y).

- DUAL SWITCHED CAPACITOR DELAY LINE
- 3MHz CLOCK DERIVED FROM 6MHz VCO LOCKED BY THE BURST GATE PULSE
- SAMPLE AND HOLD CIRCUITS AND LOW-PASS FILTERS TO SUPPRESS THE 3MHz CLOCK RESIDUAL
- CLAMPED B-Y AND R-Y INPUTS
- OUTPUT BUFFERS
- **ADJUSTMENT-FREE APPLICATION**
- DIP14 PACKAGE

PIN CONNECTIONS



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C, V_{CC} = 9V, R9 = 4.02kΩ, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY/V_{REF} (Pins 11 and 10)						
V_{CC}	Supply Voltage		8.5	9	9.5	V
I_{CC}	Supply Current			15	25	mA
P_d	Power Consumption	V_{CC} = 9V		135	240	mW
V_{int}	Internal Voltage			7		V
SAND CASTLE INPUT (Pin 6)						
FSSC	Burst Gate Frequency	No input signal	14.5	15.625	16.5	kHz
V_{TH}	Threshold Voltage (Burst Gate)		3.2	3.5	3.8	V
C_{in}	Input Capacitance				12	pF
COLOR DIFFERENCE INPUT SIGNALS (Pins 2 and 14)						
R-Y IPN	R-Y Typical Input Signal PAL & NTSC	Peak-to-peak value		525		mV_{PP}
R-Y IS	R-Y Typical Input Signal SECAM	Peak-to-peak value		1.05		V_{PP}
B-Y IPN	B-Y Typical Input Signal PAL & NTSC	Peak-to-peak value		665		mV_{PP}
B-Y IS	B-Y Typical Input Signal SECAM	Peak-to-peak value		1.33		V_{PP}
R_{in}	Input Resistance		10			kΩ
C_{in}	Input Capacitance				12	pF
V_{Clamp}	Clamping Voltage			2.7		V
I_{Clamp}	Clamping Current	$V_{in} = V_{Clamp} \pm 0.2V$		±50		µA
COLOR DIFFERENCE OUTPUT SIGNALS (Pins 3 and 4)						
B-Y O	B-Y Output Signal	Peak-to-peak value			1.8	V_{PP}
R-Y O	R-Y Output Signal	Peak-to-peak value			1.8	V_{PP}
DG	Differential Gain	SECAM V_n/V_{n-1} : V_{in} = $1V_{PP}$	-0.4	0	+0.4	dB
GPN	PAL-NTSC Gain	$V_{in} = 0.5V_{PP}$	5.8	6.3	6.8	dB
GS	SECAM Gain	$V_{in} = 1V_{PP}$	-0.5	0	+0.5	dB
V_{Noise}	RMS Noise Voltage	Ri = 300Ω BW = 10kHz to 1MHz		2		mV_{Rms}
R_{out}	Output Resistance			200		Ω
Delay	Delayed Signal Delay	Referred to non delayed output	63.93	64	64.07	µs
Non Delay	Non Delayed Signal Delay	Referred to input		100		ns
TR	Output Signal Transient Time	500ns transient input signal		650	1000	ns
PLL FILTER LOOP (Pin 5)						
I_{Charg}	Charging Current			100		µA
V_{PLL}	DC Voltage			3.5		V
CURRENT REFERENCE (Pin 9)						
V_{DC}	DC Voltage	R9 = 4.02kΩ to ground		1.15		V

STV5112

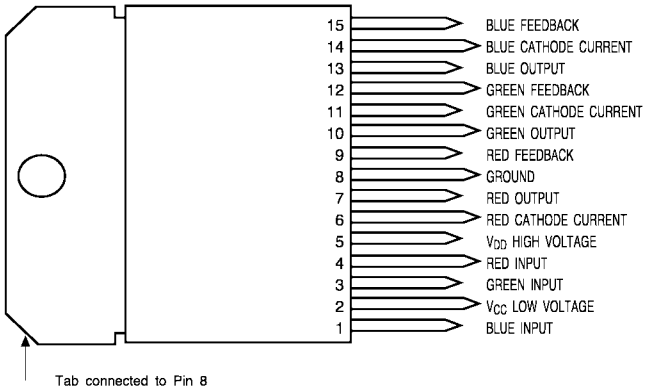
RGB HIGH VOLTAGE VIDEO AMPLIFIER

DESCRIPTION

The STV5112 includes three video amplifiers designed with a high voltage bipolar /CMOS/DMOS technology (BCD). It drives directly the three cathodes and is protected against flashovers. Thanks to its three cathode current outputs, the STV5112 can be used with both parallel and sequential sampling applications.

- BANDWIDTH : 8 MHz TYPICAL
- RISE AND FALL TIME 50ns TYPICAL
- CRT CATHODE CURRENT OUTPUTS FOR PARALLEL OR SEQUENTIAL CUT-OFF OR DRIVE ADJUSTMENT
- FLASH-OVER PROTECTION
- POWER DISSIPATION : 3.6 W

PIN CONNECTIONS (top view)



PIN FUNCTION

N	Function	Description
1	Blue Input	Input of the "blue" amplifier. It is a virtual ground with 25V bias voltage and 75µA input bias current.
2	V_{CC}	Low voltage power supply, typically 9V.
3	Green Input	Input of the "green" amplifier. It is a virtual ground with 2.5V bias voltage and 75µA input bias current.
4	Red Input	Input of the "red" amplifier. It is a virtual ground with 25V bias voltage and 75µA input bias current.
5	V_{DD}	High voltage power supply, typically 220V.
6	Red Cathode Current	Provides the video processor with a copy of the DC current flowing into the red cathode, for automatic cut-off or gain adjustment. If this control is not used, Pin 6 must be grounded.
7	Red Output	Output driving the red cathode. Pin 7 is internally protected against CRT arc discharges by a diode limiting the output voltage to V_{DD}.
8	Ground	Also connected to the heatsink.
9	Red Feedback	Output driving the feedback resistor network for the red amplifier.
10	Green Output	Output driving the green cathode. Pin 10 is internally protected against CRT arc discharges by a diode limiting the output voltage to V_{DD}.
11	Green Cathode Current	Provides the video processor with a copy of the DC current flowing into the green cathode, for automatic cut-off or gain adjustment. If this control is not used, Pin 11 must be grounded.
12	Green Feedback	Output driving the feedback resistor network for the green amplifier.
13	Blue Output	Output driving the blue cathode. Pin 13 is internally protected against CRT arc discharges by a diode limiting the output voltage to V_{DD}.
14	Blue Cathode Current	Provides the video processor with a copy of the DC current flowing into the blue cathode, for automatic cut-off or gain adjustment. If this control is not used, Pin 14 must be grounded.
15	Blue Feedback	Output driving the feedback resistor network for the blue amplifier.

STV5347/5348

MONOCHIP TELETEXT AND VPS DECODER WITH ONE INTEGRATED PAGE

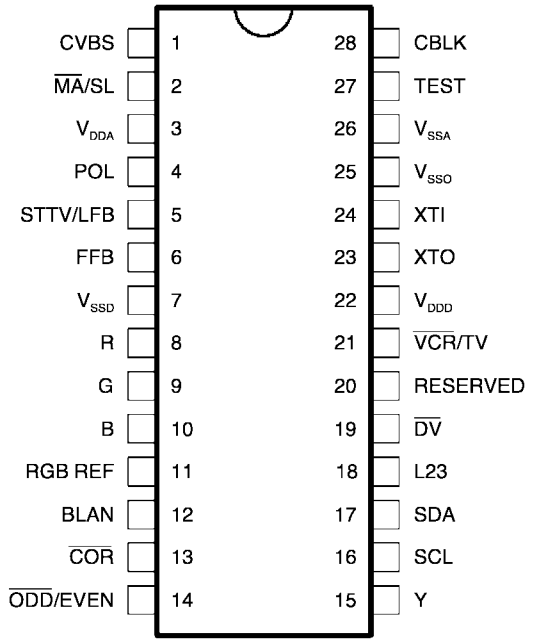
DESCRIPTION

The STV5347 teletext decoder is computer-controlled. It can store either 1 teletext page without ghost row, or 2 teletext pages with ghost rows. Data slicing and capturing extracts the teletext information embedded in the composite video signal. Control is accomplished via a two wire serial I^2C bus). Chip address is 22h. Internal ROM provides a character set suitable to display text using up to seven national languages. Hardware and software features allow selectable master/slave synchronization configurations. The STV5347 also supports facilities for reception and display of current level protocol data.

Type	Language					
STV5347/E	English	German	Swedish	Italian	French	Spanish
STV5348/T	English	German	Türkish	Italian	French	Spanish
STV5348/H	Polish	German	Swedish	Serbo-croat	Czech-Slovakian	Rumanian
STV5348/C	Estonian	Lettish /Lithuanian	Russian			

- COMPLETE TELETEXT AND VPS DECODER INCLUDING AN 1 PAGE MEMORY ON A SINGLE CHIP
- UPWARD SOFTWARE COMPATIBLE WITH PREVIOUS SGS-THOMSON's MULTICHIP SOLUTIONS (SAA5231, SDA5243, STV5345)
- PERFORM PDC SYSTEM A (VPS) AND PDC SYSTEM B (8/30/2) DATA STORAGE SEPARATLY
- DEDICATED "ERROR FREE" OUTPUT FOR VALID PDC DATA
- INDICATION OF LINE 23 FOR EXTERNAL USE
- SINGLE +5V SUPPLY VOLTAGE
- SINGLE 13.875MHz CRYSTAL
- REDUCED SET OF EXTERNAL COMPONENTS, NO EXTERNAL ADJUSTMENT
- OPTIMIZED NUMBER OF DIGITAL SIGNALS REDUCING EMC RADIATION
- HIGH DENSITY CMOS TECHNOLOGY
- DIGITAL DATA SLICER AND DISPLAY CLOCK PHASE LOCK LOOP
- 28 PIN DIP & SO PACKAGE

PIN CONNECTIONS

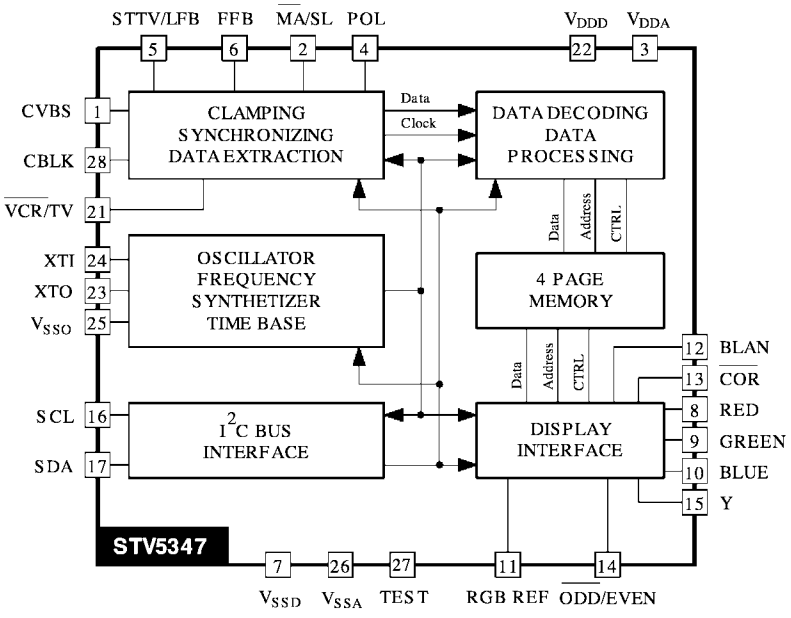


PIN DESCRIPTION

Pin N°	Symbol	Function	Description	Figure
1	CVBS	Input	Composite Video Signal Input through Coupling Capacitor	9
2	$\overline{MA}$/SL	Input	Master/Slave Selection Mode	11
3	V_{DDA}	Analog Supply	+5V	-
4	POL	Input	STTV / LFB / FFB Polarity Selection	12
5	STTV/LFB	Output / Input	Composite Sync Output, Line Flyback Input	15
6	FFB	Input	Field Flyback Input	12
7	V_{SSD}	Ground	Digital Ground	-
8	R	Output	Video Red Signal	13
9	G	Output	Video Green Signal	13
10	B	Output	Video Blue Signal	13
11	RGBREF	Supply	DC Voltage to define RGB High Level	13
12	BLAN	Output	Fast Blanking Output TTL Level	15
13	$\overline{COR}$	Output	Open Drain Contrast Reduction Output	15
14	$\overline{ODD}$/EVEN	Output	25Hz Output Field synchronized for non-interlaced display	15
15	Y	Output	Open Drain Foreground Information Output	15
16	SCL	Input	Serial Clock Input	16
17	SDA	Input/ Output	Serial Data Input/Output	17
18	L23	Output	Line 23 Identification	15
19	$\overline{DV}$	Output	VPS Data Valid	15
20	RESERVED	Test	To be connected to V_{SSD} through a resistor	15
21	$\overline{VCR}$/TV	Input	PLL Time Constant Selection	15
22	V_{DDD}	Digital Supply	+5V	-
23	XTO	Crystal Output	Oscillator Output 13.875MHz	14
24	XTI	Crystal Input	Oscillator Input 13.875MHz	14
25	V_{SSO}	Ground	Oscillator Ground	-
26	V_{SSA}	Ground	Analog Ground	-
27	TEST	Test	Grounded to V_{SSA}	11
28	CBLK	Input / Output	To connect Black Level Storage Capacitor	28

5347-01.TBL

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (V_{DD} = 5V, V_{SS} = 0V, T_A = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SUPPLIES					
V_{DD}	Supply Voltage	4.75	5	5.25	V
I_{DDD}	V_{DDD} Pin Supply Current		30		mA
I_{DDA}	V_{DDA} Pin Supply Current		5		mA
INPUTS					
CBLK					
I_{BLKO}	Source Current (V_{CBLK} = 2V, V_{CVBS} = 0V)		80		µA
I_{BLKI}	Sink Current (V_{CBLK} = 2V, V_{CVBS} = 1V))		- 10		µA
CVBS					
CVBSI	Video Input Amplitude (peak to peak)		1		V
CVBSC	Input Capacitance			10	pF
t_{SYNC}	Delay from CVBS to TCS Output from STTV Pin		200		ns
V_{CLAMP}	Clamping Level at Synchro Pulse		0		mV
I_{CLPH}	High Level Clamp Current (CVBS = V_{CLAMP} + 1V)		5		µA
I_{CLPL}	Low Level Clamp Current (CVBS = V_{CLAMP} - 0.3V)		- 400		µA
$\overline{MA}$/SL, POL, LFB, FFB, $\overline{VCR}$/TV					
V_{IL}	Input Voltage Low Level	- 0.3		+ 0.8	V
V_{IH}	Input Voltage High Level	2		V_{DD}	V
I_{IL}	Input Leakage Current (V_I = 0 to V_{DDD})	- 10		+ 10	µA
C_I	Input Capacitance			10	pF
SCL, SDA					
V_{IL}	Input Voltage Low Level	- 0.3		+ 1.5	V
V_{IH}	Input Voltage High Level	3		V_{DD}	V
I_{IL}	Input Leakage Current (V_I = 0 to V_{DD})	- 10		+ 10	µA
f_{SCL}	Clock Frequency (SCL)			100	kHz
t_R, t_F	Input Rise and Fall Time (10 to 90%)			2	µs
C_I	Input Capacitance			10	pF
RGB REF					
V_I	Input Voltage	- 0.3		V_{DD}	V
I_I	Input Current			50	mA

ELECTRICAL CHARACTERISTICS - V_{DD} = 5V, V_{SS} = 0V, T_A = 25°C (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
OUTPUTS					
RGB					
V_{OL}	Output Low Voltage (I_{OL} = 2mA)			0.4	V
V_{OH}	Output High Voltage (I_{OH} = -2mA, RGB REF = V_{DD}/2)	RGB REF - 0.5		RGB REF	V
C_L	Load Capacitance			50	pF
t_R, t_F	Rise and Fall Time (10 to 90%)			20	ns
BLAN					
V_{OL}	Output Low Voltage (I_{OL} = 2mA)	0		0.4	V
V_{OH}	Output High Voltage (I_{OH} = -0.2mA)	V_{DD} - 0.5			V
C_L	Load Capacitance			50	pF
t_R, t_F	Rise and Fall Time (10 to 90%)			20	ns
$\overline{ODD}$/EVEN, STTV, L23, $\overline{DV}$					
V_{OL}	Output Low Voltage(I_{OL} = 2mA)	0		0.5	V
V_{OH}	Output High Voltage (I_{OH} = -0.2mA)	V_{DD} - 0.8		V_{DD}	V
C_L	Load Capacitance			50	pF
t_R, t_F	Rise and Fall Time (10 to 90%)			20	ns
$\overline{COR}$ AND Y (with Pull up to V_{DDD})					
V_{OL}	Output Low Voltage (I_{OL} = 2mA)	0		0.5	V
C_L	Load Capacitance			25	pF
t_F	Fall Time (R_L = 1.2kΩ, V_{DDD} - 0.5V to 1.5V)			50	ns
I_{OLL}	Output Leakage Current	-10		+10	µA
SDA					
V_{OL}	Output Low Voltage (I_{OL} = 3mA)	0		0.5	V
t_F	Fall Time (3.0 to 1.0V)			200	ns
C_L	Load Capacitance			400	pF
CRYSTAL OSCILLATOR					
XTI, XTO					
f_{XTAL}	Crystal Frequency		13.875		MHz
R_{BIAS}	Internal Bias Resistance	0.4	1	3	MΩ
C_I	Input Capacitance			7	pF
TIMING					
SERIAL BUS (referred to V_{IH} = 3V, V_{IL} = 1.5V)					
t_{LOW} t_{HIGH}	Clock : ● Low Period ● High Period	 4 4			µs
$t_{SU, DAT}$	Data Set-up Time	250			ns
$t_{HD, DAT}$	Data Hold Time	170			ns
$t_{SU, STO}$	Stop Set-up Time from Clock High	4			µs
t_{BUF}	Start Set-up Time following a Stop	4			µs
$t_{HD, STA}$	Start Hold Time	4			µs
$t_{SU, STA}$	Start Set-up Time following Clock Low to High Transition	4			µs

STV8225

AM SIF CIRCUIT

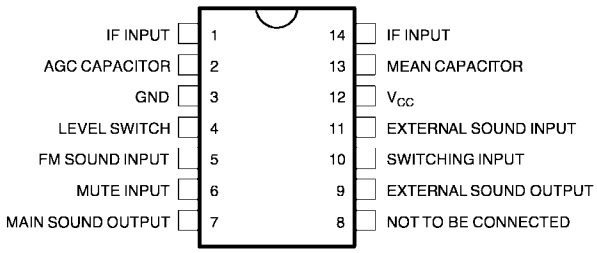
DESCRIPTION

The STV8225 is intended for the demodulation of the AM sound of the L standard.

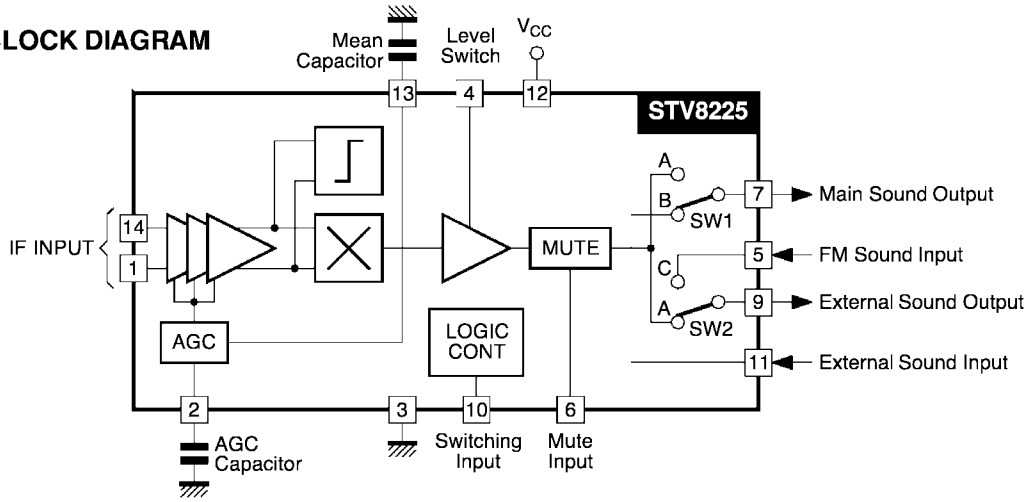
Used as an add on to the STV8224 it permits to design a multistandard set with the needed switches for one SCART plug.

- SOUND AM SYNCHRONOUS DEMODULATOR
- AM/FM AUDIO SWITCH
- AV/TV AUDIO SWITCH
- MUTE INPUT

PIN CONNECTIONS



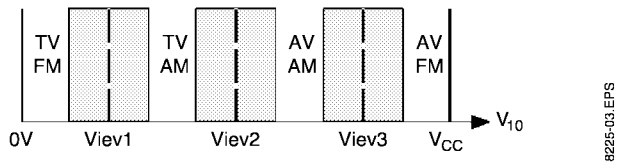
BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (V_{CC} = 9V, V_{IN} = 10mV$_{RMS}$, f_{OSC} = 32.4MHz, f_M = 1kHz, m = 54% modulation depth, Audio BW = 40Hz to 15kHz, T_{amb} = 25°C,

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	Pin 12	8	9	10	V
I_{CC}	Supply Current	Pin 12		20	30	mA
	Supply Voltage Rejection	Pins 9, 7, 12 - V_{Ripple} = 0.5V$_{PP}$, f = 100Hz	45	53		dB
IF AMPLIFIER						
Ri 1, 14	Input Resistance (Pins 1-14)	Resistance between Pin 1 and 14		2		kΩ
Ci 1, 14	Input Capacitance (Pins 1-14)	Capacitance between Pin 1 and 14		2		pF
VIF min	Minimum IF Input Signal	IF input signal for V_{OUT} = V_{NOM} - 3dB		70		μV_{RMS}
VIF max	Maximum IF Input Signal	IF input signal for V_{OUT} = V_{NOM} + 1dB		75		mV_{RMS}
DAV	AGC Range	DAV = VIF max / VIF min		61		dB
I_{AGC}	Maximum AGC Output Current (Pin 2)	Charging and discharging	±35	± 50	± 65	µ A
	IF Bandwidth	-3dB		50		MHz

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 9V, V_{IN} = 10mV_{RMS}, f_{SC} = 32.4MHz, f_M = 1kHz, m = 54% modulation depth, Audio BW = 40Hz to 15kHz, T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AM DEMODULATOR						
	AF Output Voltage (Pins 7-9)	Level switch (Pin 4) open Level switch (Pin 4) connected to GND	200 400	250 500	300 600	mV_{RMS} mV_{RMS}
	AF Bandwidth (Pins 7-9) Lower Limit Upper Limit	-3dB versus nominal signal	 50		40	 Hz kHz
	Harmonic Distorsion (Pins 7-9)	THD + Noise		0.7	1.8	%
	S/N (Pins 7-9)	Weighted according to CCIR 468-4		55		dB
MUTE						
	Threshold Level (Pin 6)	Mute mode if voltage below threshold	0.2	0.3	0.4	V
	Attenuation (Pins 7-9)	Level switch (Pin 4) connected to GND TV - AM mode	80	96		dB
AUDIO SWITCHES						
	Switching Voltage (Pin 10)	Operation mode 				
View1	Level 1 (Pin 10)	For voltage below this level TV-FM mode : Pin 7 connected to A Pin 9 connected to C	1.8	2.3	2.6	V
View2	Level 2 (Pin 10)	For voltage below this level TV-AM mode : Pin 7 connected to A Pin 9 connected to A	4.1	4.6	4.9	V
View3	Level 3 (Pin 10)	For voltage below this level AV-AM mode : Pin 7 connected to B Pin 9 connected to A For voltage above this level AV-FM mode : Pin 7 connected to B Pin 9 connected to C	6.4	6.8	7.2	V
	Input Current (Pin 10)	Source current		0.3	2	µA
	Input Dynamic Range (Pins 5-11)		2			V_{RMS}
	Input Resistance (Pins 5-11)		35	50		kΩ
	Switch Gain	V_{IN} = 2V_{RMS}, f = 1kHz Pin 7 vs Pin 11 and Pin 9 vs Pin 5	-0.6	-0.1	0.4	dB
	Crosstalk	f = 1kHz	70	85		dB
	Output Resistance (Pins 7-9)		70	100	130	Ω
	Output Current Source (Pins 7-9)			1		mA
	Switch Distorsion	V_{IN} = 2V_{RMS}, f = 1kHz, THD + Noise, Pin 7 vs Pin 11 and Pin 9 vs Pin 5		0.1	0.5	%
	Output Noise	Unweighted		7	20	µVp
	DC Plop at AF Output Pin			10	50	mV

TDA2822

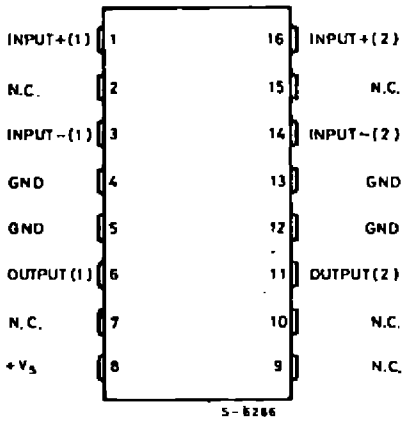
DUAL POWER AMPLIFIER

- SUPPLY VOLTAGE DOWN TO 3 V
- LOW CROSSOVER DISTORSION
- LOW QUIESCENT CURRENT
- BRIDGE OR STEREO CONFIGURATION

DESCRIPTION

The TDA2822 is a monolithic integrated circuit in 12+2+2 powerdip, intended for use as dual audio power amplifier in TV sets.

PIN CONNECTION (top view)



ELECTRICAL CHARACTERISTICS (V_s = 6 V, T_{amb} = 25 °C,

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		3		15	V
V_c	Quiescent Output Voltage	V_s = 9 V V_s = 6 V		4 2.7		V V
I_d	Quiescent Drain Current			6	12	mA
I_b	Input Bias Current			100		nA
P_o	Output Power (each channel)	d = 10 % f = 1 kHz V_s = 9 V R_L = 4 Ω V_s = 6 V R_L = 4 Ω V_s = 4.5 V R_L = 4 Ω	 1.3 0.45	 1.7 0.65 0.32		 W W W
G_v	Closed Loop Voltage Gain	f = 1 kHz	36	39	41	dB
R_i	Input Resistance	f = 1 kHz	100			kΩ
e_N	Total Input Noise	R_s = 10 kΩ B = 22 Hz to 22 kHz Curve A		2.5 2		µV µV
SVR	Supply Voltage Rejection	f = 100 Hz	24	30		dB
CS	Channel Separation	R_g = 10 kΩ f = 1 kHz		50		dB

BRIDGE (test circuit of fig. 2)

V_s	Supply Voltage		3		15	V
I_d	Quiescent Drain Current	R_L = °		6	12	mA
V_{os}	Output Offset Voltage	R_L = 8 Ω		10	60	mV
I_b	Input Bias Current			100		nA
P_o	Output Power	d = 10 % f = 1 kHz V_s = 9 V R_L = 8 Ω V_s = 6 V R_L = 8 Ω V_s = 4.5 V R_L = 4 Ω	 2.7 0.9	 3.2 1.35 1		 W W W
d	Distortion (f = 1 kHz)	R_L = 8 Ω P_o = 0.5 W		0.2		%
G_v	Closed Loop Voltage Gain	f = 1 kHz		39		dB
R_i	Input Resistance	f = 1 kHz	100			kΩ
e_N	Total Input Noise	R_s = 10 kΩ B = 22 Hz to 22 kHz Curve A		3 2.5		µV µV
SVR	Supply Voltage Rejection	f = 100 Hz		40		dB

TDA8174

VERTICAL DEFLECTION CIRCUIT

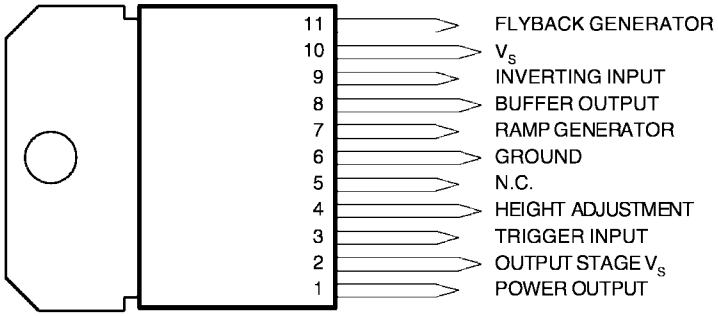
- RAMP GENERATOR
- INDEPENDENT AMPLITUDE ADJUSTMENT
- BUFFER STAGE
- POWER AMPLIFIER
- FLYBACK GENERATOR
- INTERNAL REFERENCE VOLTAGE
- THERMAL PROTECTION

DESCRIPTION

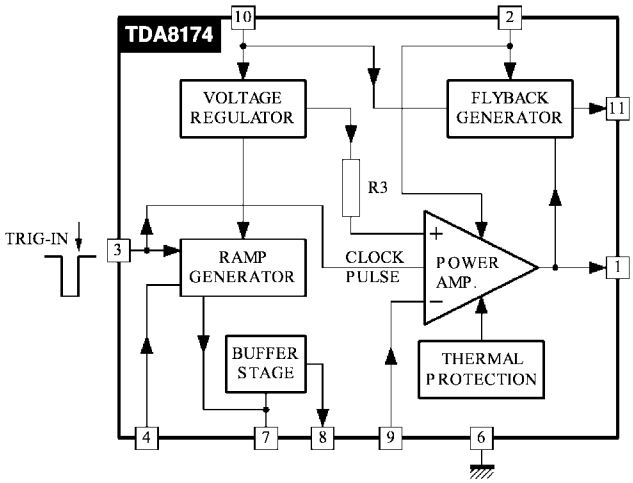
TDA8174 and TDA8174W are a monolithic integrated circuits.

It is a full performance and very efficient vertical deflection circuit intended for direct drive of a TV picture tube in Color and B & W television as well as in Monitor and Data displays.

PIN CONNECTIONS (top view)



BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS (V_S = 35V ; T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_2	Pin 2 Quiescent Current	I_1 = 0, I_{11} = 0		16	36	mA
I_{10}	Pin 10 Quiescent Current	I_1 = 0, I_{11} = 0		15	30	mA
—I	Ramp Generator Bias Current	V_7 = 0			0.5	µA
—I	Ramp Generator Current	V_7 = 0, —I = 20µA	18.5	20	21.5	µA
dI_7/I_7	Ramp Generator Linearity	V_6 = 0 to 15V, —I = 20µA		0.2	1	%
V_1	Quiescent Output Voltage	R_a = 30kΩ, R_b = 10kΩ, V_s = 35V	17.0	17.8	18.6	V
		R_a = 6.8kΩ, R_b = 10kΩ, V_s = 15V	7.2	7.5	7.8	V
V_{1L}	Out Saturation Voltage to GND	I_1 = 0.5A		0.5	1	V
		I_1 = 1.2A		1	1.4	V
V_{1H}	Out Saturation Voltage to V_s	—I = 0.5A		1.1	1.6	V
		—I = 1.2A		1.6	2.2	V

DC ELECTRICAL CHARACTERISTICS (continued

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_4	Reference Voltage	—I = 20µA	6.3	6.6	6.9	V
dV_4/V_s	Reference Voltage Drift Versus V_s	V_s = 10V to 35V		1	2	mV/V
dV_4/dI_4	Reference Voltage Drift Versus I_4	I_4 = 10µA to 30µA		1.5	2	mV/µA
V_r	Internal Reference Voltage		4.26	4.40	4.54	V
V_{D11-10}	Diode Fwd Voltage	I_D = 1.2A		2.2	3	V
V_{D1-2}	Diode Fwd Voltage	I_D = 1.2A		2.2	3	V
G_V	Output Stage Open Loop Gain	f = 100Hz		60		dB
V_{fs}	V_{10-11} Saturation Voltage	—I = 1.2A		1.5	2.5	V
V_{11}	Pin 11 Scanning Voltage	I_{11} = 20mA		1.7	3	V
V_3	Trigger Input Threshold	(see note 1)	2.6	3.0	3.4	V
I_3	Trigger Input Bias Current	V_{IN} = V_3- 0.2V			30	µA
t_3	Trigger Input Width	(see note 2)	20	60	Th	µS

Notes : 1. The trigger input circuit can accept, with a metal option, positive and negative going input pulses.

2. $Th = \frac{1.2 \varsigma T_S}{V_{PP}}$ where : T_S is the vertical period and V_{PP} is ramp amplitude at Pin7

AC ELECTRICAL CHARACTERISTICS (V_S = 24V ; T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Operating Supply Voltage Range		10		30	V
I_1	Peak-to-peak Operating Current Range		0.4			A
I_s	Supply Current	I_y = 2.4A_{pp}		315		mA
V_1	Flyback Voltage	I_y = 2.4A_{pp}		51		V
V_8	Sawtooth Pedestall Voltage			1.85		V
T_{js}	Junction Temp. for Thermal Shutdown			145		ϒC

SERVICE ADJUSTMENTS

1-Supply Voltage adjustment

Connect a digital voltmeter to the anode of D950 and set the screen potentiometer to minimum. Adjust the main supply voltage +B with P901 to following voltage values;

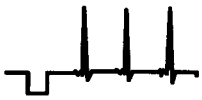
113V DC for 14" IRICO tube,
107V DC for 14" PHILIPS tube,
104V DC for 14" LG tube,
121V DC for 20" SAMSUNG tube,
117V DC for 20" LG tube,
113V DC for 21" LG tube,
119V DC for 21" SAMSUNG tube,

Adjust the screen potentiometer to the level where a picture is just visible. Adjust the focus potentiometer.

2- AFC adjustment

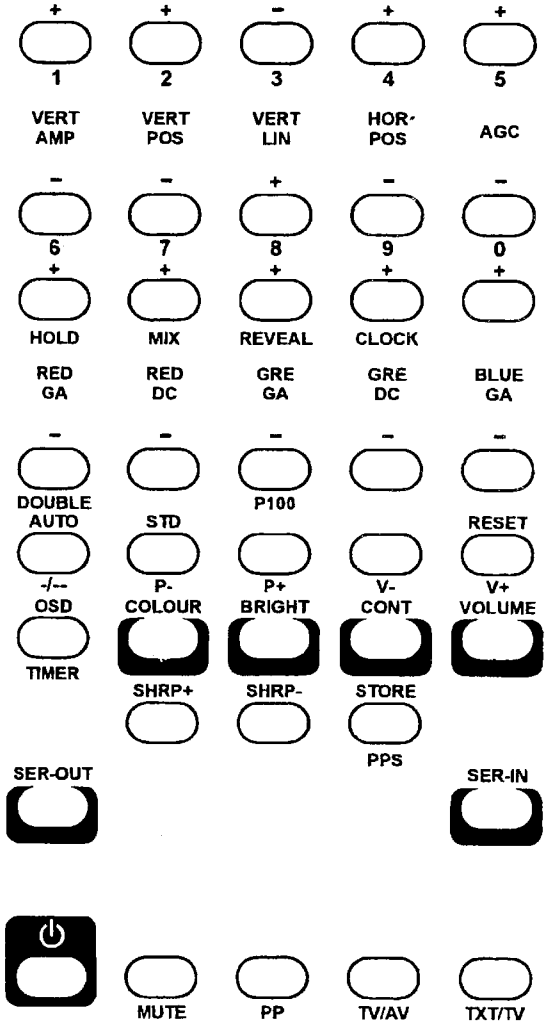
Press Yellow button then TVTX button to call the tuning table. Press Yellow button again to set the AFC to OFF. Apply a crosshatch pattern with 38.9 IF carrier to pins 1-2 of F105. Connect the oscilloscope to the video output pins of the scart connector. Adjust L101 until the waveform on the oscilloscope Fig 1 is visiable and the voltage at PIN 9 of IC 401 becomes 2,425 V + - 75mV. Video output level at scart output should be 2Vpp.

Figure 1



Set the AFC ON again in menu.

SERVICE REMOTE CONTROL:



3- AGC adjustment

Apply a signal at CH32 with 60±dBuV level to the antenna input. Enter the Service Mode, using "Ser IN" button on service RC. Using "AGC" buttons adjust the voltage at the AGC pin of Tuner to 4 V + - 50mV DC. Press "PPS" to store the adjusted values.

4- Sharpness adjustment

Set the XY value (sharpness adjustment) to 4 by using 'SHRP + 'and' SHRP - 'buttons on service RC.

Apply an AV signal from Scart (Video in (20) and Audio in (2 and 6)) inputs of CHASSIS and then observe a clear picture and sound.

5- Geometry adjustment

Apply a FUBK or Philips test pattern.
For Vertical Linearity, use buttons "2" and "7".
For Vertical Position, use buttons "3" and "8".
For Vertical Amplitude, use buttons "1" and "6".
For Horizontal Position, use buttons"4" and "9".

There is no Horizontal width adjustment. If this adjustment is necessary this can be done changing the mains voltage ± 1V.

6- Screen adjustment

Set the TV to AV mode when Brightness (%55), Contrast (%80), and Color (%55) are at their stored values. Connect a digital voltmeter to PIN10 of IC801. Adjust the screen potentiometer by increasing the voltage from 0 to 105 ± 1V.

7- White balance adjustment

Apply a Grey Scale test pattern. There is no blue cut-off adjustment (low light) at white adjustment. Set the G-Gain value to 45 using"G-Gain+" and "G-Gain-" buttons. Then perform white adjustment by using,
Red high light increase/decrease (R-Gain +/-) buttons.
Blue high light increase/decrease (B-Gain +/-) buttons.
Red low light increase/decrease (R-DC +/-) buttons.
Green low light increase/decrease (G-DC +/-) buttons.

Set the colour system to "Auto" using "P-/STD" button.

OSD colour bars can be seen by using "Timer/OSD" for OSD control.

Always, use "SER.IN" button to enter the Service Menu and "SER.OUT" button to exit the Service Menu. In order to store press "STORE" button to store above adjusted values.

See attached table for Geometry and White Balance settings.

THE VALUES WILL BE PRESET ACCORDING TO THE TUBES:

White adjustment 9300 K (0)
High Light 60 Nits Low Light 6 Nits

1-) IRICO TUBE :

For a PAL Broadcast:		**For a NTSC Broadcast:**		**RGB Values:**	
VER. AM.	:15	VER. AM.	:27	R-Gain	:50
VER. POS.	:03	VER. POS.	:04	B-Gain	:55
VER. LIN.	:08	VER. LIN.	:08	G-Gain	:45
HOR. POS.	:37	HOR. POS.	:37	R-DC	:45
				G-DC	:35

2-) PHILIPS TUBE :

For a PAL Broadcast:		**For a NTSC Broadcast:**		**RGB Values:**	
VER. AM.	:16	VER. AM.	:26	R-Gain	:50
VER. POS.	:02	VER. POS.	:04	B-Gain	:55
VER. LIN.	:10	VER. LIN.	:10	G-Gain	:45
HOR. POS.	:37	HOR. POS.	:37	R-DC	:45
				G-DC	:35

3-) LG TUBE :

For a PAL Broadcast:		**For a NTSC Broadcast:**		**RGB Values:**	
VER. AM.	:19	VER. AM.	:28	R-Gain	:50
VER. POS.	:03	VER. POS.	:04	B-Gain	:55
VER. LIN.	:08	VER. LIN.	:08	G-Gain	:45
HOR. POS.	:36	HOR. POS.	:36	R-DC	:45
				G-DC	:35

1-) SAMSUNG TUBE : 20"

For a PALI Broadcast:		**For a NTSC Broadcast:**		**RGB Values:**	
VER. AM.	:28	VER. AM.	:45	R-Gain	:50
VER. POS.	:01	VER. POS.	:03	B-Gain	:55
VER. LIN.	:33	VER. LIN.	:33	G-Gain	:45
HOR. POS.	:45	HOR. POS.	:45	R-DC	:45

2-) LG TUBE : 20"

For a PAL Broadcast:		**For a NTSC Broadcast:**		**RGB Values:**	
VER. AM.	:25	VER. AM.	:40	R-Gain	:50
VER. POS.	:03	VER. POS.	:05	B-Gain	:55
VER. LIN.	:15	VER. LIN.	:15	G-Gain	:45
HOR. POS.	:42	HOR. POS.	:42	R-DC	:45

These are the main values. Geometry and white adjustments will be corrected according to standarts by entering the service mode when needed.

PIN VOLTAGES OF INTEGRATED CIRCUITS

1. SWITCH-MODE CIRCUIT AND IC901 PIN VOLTAGES

IC901 Pin No.	Stand-By Mode			Operation Mode		
	DC (V)	AC	NOTES	DC (V)	AC	NOTES
1	12V			12.7		
2	12.4			12.2		
3	0.2			1.7		
4	—			—		
5	2.8V			3.1V		
6	—			—		
7	—			—		
8	0.1			0.1		
9	—			—		
10	2.6			2.6		
11	2.4			2.4		
12	1.3			0.5		
13	1.8			2.7		
14	2.5			2.5		
15	2.5			2.5		
16	2.5			2.5		
D906	—			13V		

Note1: Before these measurements, check if there is +300 VDC ~+330 DVC at pin 1 of TR901.

Note2: Be careful while making measurements never use cold chassis while the measurements are being made.

Note3: Use measurement instrument that has high internal impedance.

2- PIN VOLTAGES OF "STV8223B" IC101 IF FREQUENCY IC.

Pin No.			NOTES
	DC (V)	AC (V)	
1	1.9		
2	4.7		
3	2.5		
4	0		
5	5.9		
6	5.9		
7	4.8		
8	3.8		
9	4.5		
10	2.3		
11	2.5		
12	1.8		
13	0.4		
14	4.4		
15	4.5		
16	4.5		
17	9.2		
18	0		
19	2.9		
20	2.9		
21	3.3		
22	4.0		
23	2.3		
24	0.6		

3- PIN VOLTAGES OF "ST6387" (IC401) CPU

Pin No.	DC (V)	AC	Pin No.	DC (V)	AC)
1	5.0		22	0	
2	1.1		23	0	
3	2.2		24	0	
4	2.2		25	0	
5	0.1		26	0.9	
6	2.1		27	0.2	
7	0		28	4.9	
8	1.3		29	4.9	
9	2.2		30	0	Stops while operating.
10	4.9		31	—	
11	0		32	—	
12	0		33	4.3	
13	4.9		34	2.1	
14	4.9		35	4.9	
15	4.9		36	0	
16	4.9		37	7.9	
17	4.7		38	0.4	
18	4.7		39	1.3	
19	9.2		40	3.8	
20	0		41	2.8	
21	0		42	4.9	

4. PIN VOLTAGES OF (IC 151) "STV2116A" COLOUR AND RGB INPUT/OUTPUT IC.

Pin No.	DC (V)	AC (V)	Pin No.	DC (V)	AC (V)
1	0		22	9.2	
2	8.3		23	0	
3	3.8		24	2.2	
4	4.8		25	2.0	
5	3.5		26	2.1	
6	3.8		27	1.9	
7	2.8		28	2.1	
8	4.6		29	1.8	
9	0		30	2.1	
10	0.6		31	6.7	
11	0		32	2.5	
12	1.5		33	4.5	
13	1.4		34	4.5	
14	1.4		35	5.4	
15	0		36	2.9	
16	1.8		37	0.6	
17	1.6		38	2.7	
18	1.6		39	2.9	
19	0		40	5.7	
20	4.0		41	5.6	
21	0		42	9.1	

5- PIN VOLTAGES OF SECAM CONVERTER AND DELAY LINE "STV2180A" IC.					
Pin No.			Pin No.		
	DC (V)	AC (V)		DC (V)	AC (V)
1		0	8		0
2		2.5	9		1.1
3		3.1	10		6.8
4		3.1	11		9.0
5		3.9	12		0
6		0.6	13		0
7		0	14		2.5

6- PIN VOLTAGES OF STV5112 IC 801 RGB OUTPUT IC.				
Pin No.	Function	DC (V)	AC (V) (By oscilloscope)	NOTES
1	Blue Input	2.4		
2	Vcc (16 V)	9.0		
3	Green Input	2.5		
4	Red Input	2.5		
5	VDD (+185 V Input)	+185		
6	Red Cathode Current	3.0		
7	Red Output	107		Changes according to the picture
8	Chassis (Ground)	-		
9	Red Feedback	110		Changes according to the picture
10	Green Output	118		Changes according to the picture
11	Green Cathode Current	2.1		
12	Green Feedback	122		Changes according to the picture
13	Blue Output	120		Changes according to the picture
14	Blue Cathade Current	2.2		
15	Blue Feedback	121		Changes according to the picture

7- PIN VOLTAGES OF "STV5347" TELETEXT IC.

Pin No.	DC (V)	AC (V)	Pin No.	DC (V)	AC (V)
1	0.3		15	0	
2	0		16	2.4	
3	4.9		17	3.7	
4	0		18	0	
5	4.5		19	4.9	
6	0		20	0	
7	0		21	4.9	
8	0.4		22	4.9	
9	0.7		23	2.4	
10	0.8		24	—	Can not be measured passing channel picture
11	4.9		25	0	
12	4.7		26	0	
13	0.2		27	0	
14	24		28	1.2	

8- PIN VOLTAGES OF "TDA2822" (IC301) AUDIO OUTPUT IC.

Pin No.	DC (V)	AC (V)	Pin No.	DC (V)	AC (V)
1	0		9	0	
2	0		10	0	
3	0.5		11	5.8	
4	0		12	0	
5	0		13	0	
6	5.8		14	0.5	
7	0		15	0.2	
8	12.8		16	0	

9. VERTICAL OUTPUT STAGE AND "TDA8174A" (IC501) PIN VOLTAGES

Pin No.	Function	Operation Mode	
		DC (V)	AC (V) (By Oscilloscope)
1	Vert. Deflection Output	+ 12V	
2	Output Stage Vs	25V	
3	Trigger Input	5.2	
4	Amplitude	4.6	
5	Vertical Reference	1.5	
6	Chassis		
7	Ramp Generator	4.6	
8	Vert. Amp. Driver	5.6	
9	Inverting Input	4.4	
10	Mains Voltage	25	
11	Flyback Generator	1.1	

PIN VOLTAGES OF TRANSISTORS

1- Tuner Band Control Transistors:

Transistor Name	UHF is in use			UHF out of use			UHF is in use			UHF out of use			UHF is in use			UHF out of use		
	B(V)	E(V)	C(V)	B(V)	E(V)	C(V)	B(V)	E(V)	C(V)	B(V)	E(V)	C(V)	B(V)	E(V)	C(V)	B(V)	E(V)	C(V)
T452	4	4.7	4.7	4.5	4.7	0												
T453							4	4.7	4.7	4.7	4.7	0						
T454													4	4.7	4.7	4.7	4.7	0

2- Varicap Voltage Control Transistor

Transistor Name		VHF1		VHF3		UHF	
		Start of Band	End of Band	Start of Band	End of Band	Start of Band	End of Band
T451	E (V)	0	0	0	0	0	0
	B (V)	0.6	0	0.6	0	0.6	0
	C (V)	0	29	0	29	0	29

3- LED Switch transistor

Transistor Name	TV is in Stand- By Mode			TV is Operating		
	E (V)	B (V)	C (V)	E (V)	B (V)	C (V)
T402	1.1	0.5	0	5	2.2	0

4- Reset transistor

Transistor Name	TV is in Stand- By Mode			TV is Operating		
	E (V)	B (V)	C (V)	E (V)	B (V)	C (V)
T403				4.36	3.72	4.35

5- Vertical Output IC (K501) Control Transistors

Transistor No	TV is Normal			Geometry Adjustments are destroyed or there is a defect.			NOTES
	E (V)	B (V)	C (V)	E (V)	B (V)	C (V)	
T 501	0	0.6	0				Measurements are made when the geometry adjustments on the screen are exactly right.
T 502	5.2	5.7	11.5				

6- Horizontal Output Driver Transistor

Transistor No	E (V)	B (V)	C AC (V)	NOTES
T551	–	0.3	9	The measurement that is made while the TV is in normal operation

7- CVBS Driver and Impedance Adapter

Transistor No	E (V)	B (V)	C (V)	NOTES
T101	1.9	0.1.3	–	

8- External Scart CVBS, Video and Audio Input Control Transistors

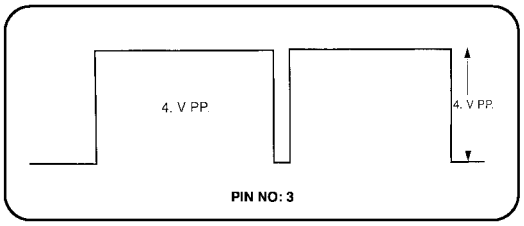
Transistor No	E (V)	B (V)	C (V)
T131-BC848B External Sound Control	3.8	4.4	4.8
T130-BC848B External CVBS Control	1.8	2.5	4.8

NOTE: Voltages of T552-BU508DF1 transistor are not given here for safety of your measurement instruments.

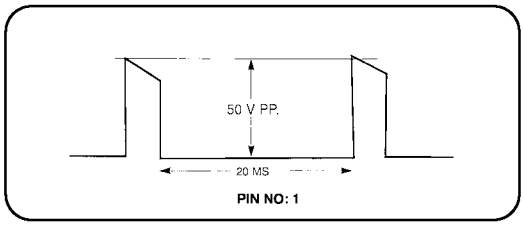
9-"Pop" Sound Cutting Circuit While The TV is Being Switched On-Off

Transistor No	E (V)	B (V)	C (V)	NOTES
T302	0	0.65	0	
T301	0	0	0	

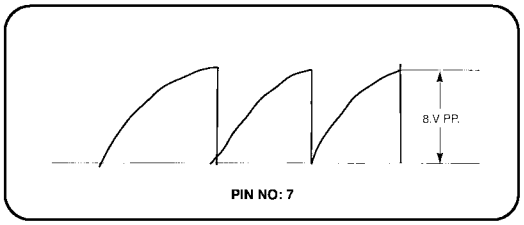
IC501 TDA 8174A
OSCILLOSCOPE WAVE FORMS



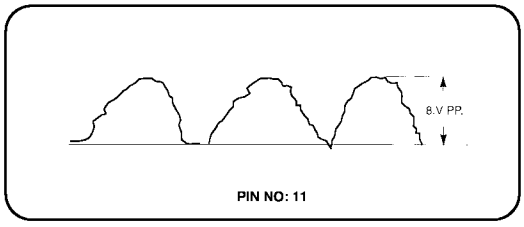
PIN NO: 3



PIN NO: 1

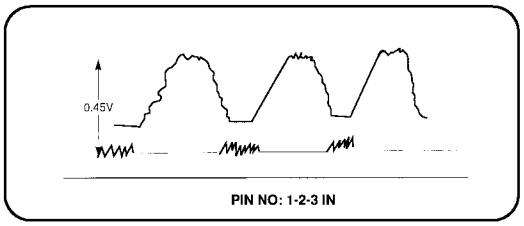


PIN NO: 7



PIN NO: 11

IC801 STV5112
OSCILLOSCOPE WAVE FORMS



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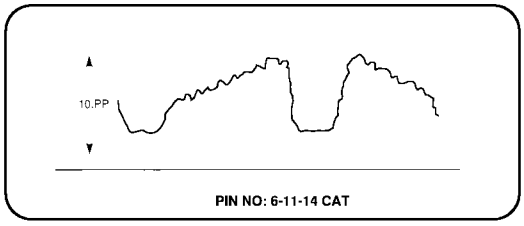

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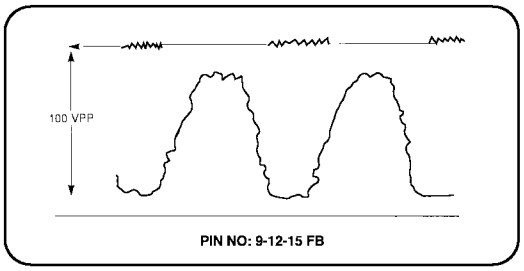
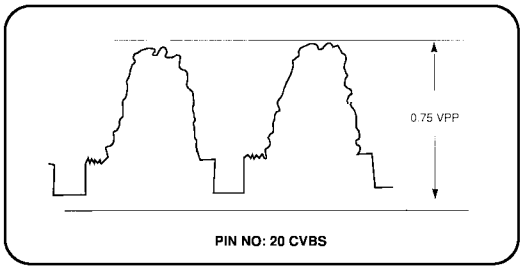


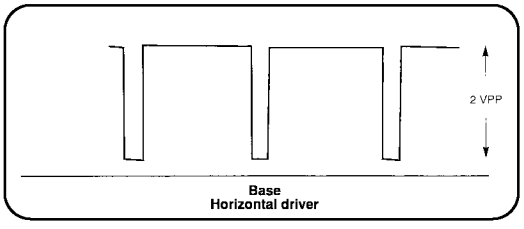
PIN NO: 9-12-15 FB

IC151 STV2116A
OSCILLOSCOPE WAVE FORMS

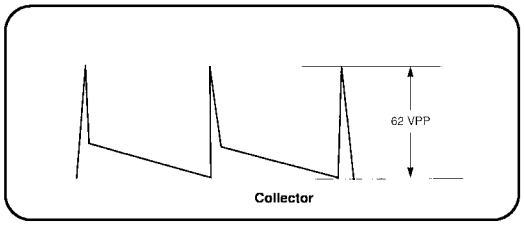


PIN NO: 20 CVBS

T551 TRN BC618
OSCILLOSCOPE WAVE FORMS

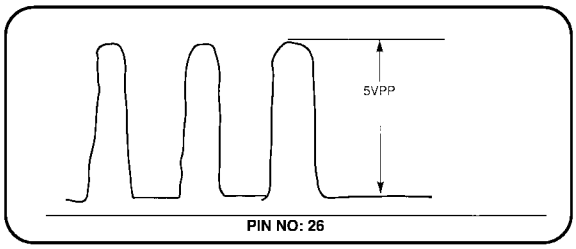


Base
Horizontal driver

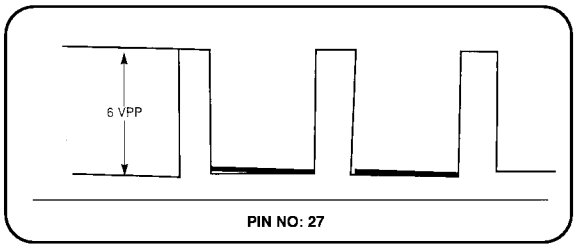


Collector

IC401 ST6387
OSCILLOSCOPE WAVE FORMS



PIN NO: 26



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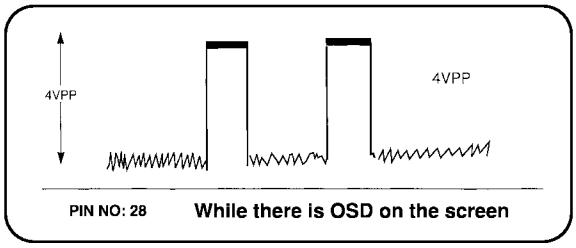
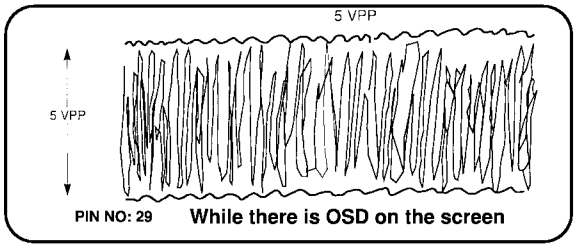
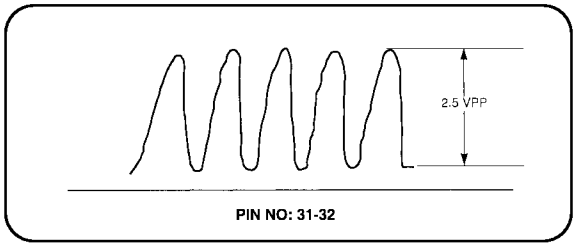


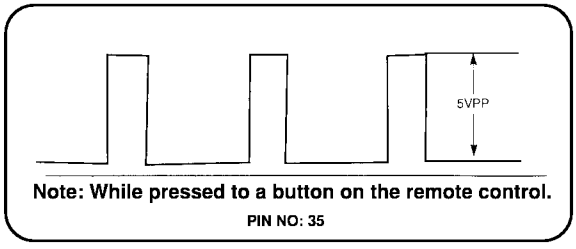
PIN NO: 28 While there is OSD on the screen



PIN NO: 29 While there is OSD on the screen

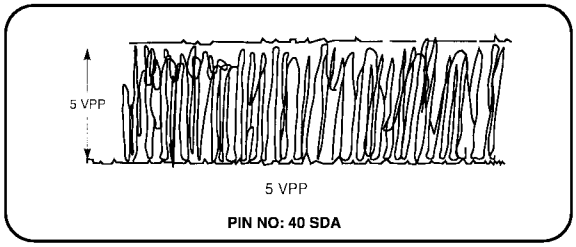


PIN NO: 31-32

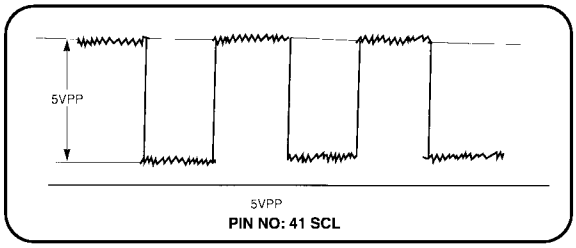


Note: While pressed to a button on the remote control.

PIN NO: 35

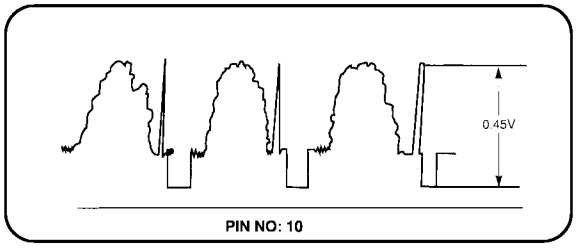


PIN NO: 40 SDA

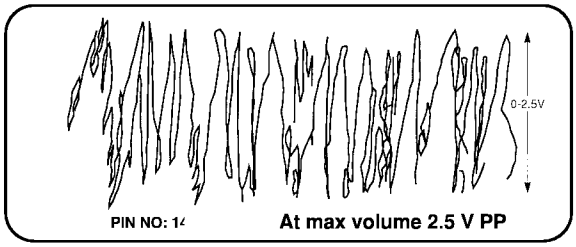


PIN NO: 41 SCL

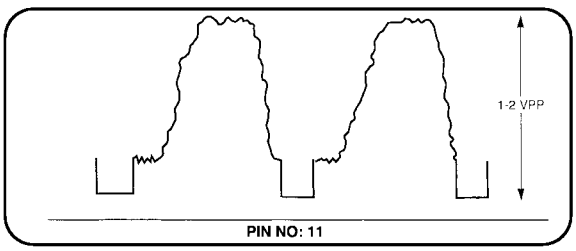
IC101 STV8223B
OSCILLOSCOPE WAVE FORMS



PIN NO: 10



PIN NO: 1< At max volume 2.5 V PP



PIN NO: 11

CONVERGENCE ADJUSTMENTS

Note: Before attempting any convergence adjustments, the receiver should be operated for at least fifteen minutes.

• Centre Convergence Adjustment

1. Receive crosshatch pattern with a colour bar signal generator.
2. Adjust the BRIGHTNESS and CONTRAST Controls for well defined pattern.
3. Adjust two tabs of the 4-Pole Magnets to change the angle between them (See figure 16) and superimpose red and blue vertical lines in the centrel area of the picture screen. (See figure).
4. Turn the both tabs at the same time keeping the constant angle to superimpose red and blue horizontal lines at the centre of the screen. (See figure)
5. Adjust two tabs of 6-Pole Magnets to superimpose red/blue line and green one. Adjusting the angle affects the vertical lines and rotating both magnets affects the horizontal lines.
6. Repeat adjustments 3,4,5 to ensure best convergence, the adjustment must be undertaken with great care because of the interaction between 4 and 6 pole magnets.

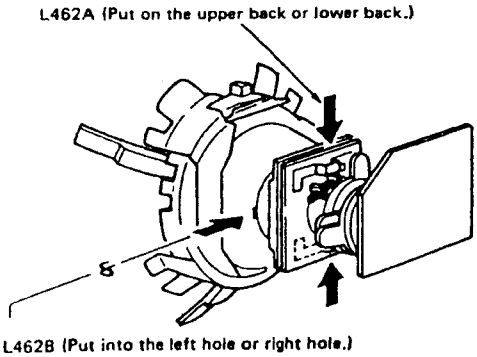
• Circumference Convergence Adjustment

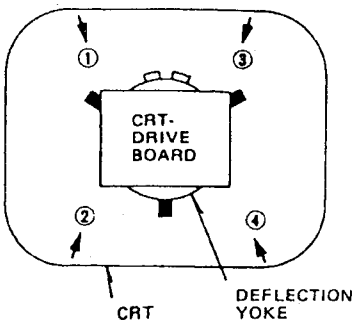
1. Loosen the clamping screw of deflection yoke to allow the yoke to tilt.
2. Put a wedge as shown in figure 15 temporarily. (Do not remove cover paper on adhesive part of the wedge.)
3. Tilt front of the deflection yoke up or down to obtain better convergence in circumference. (See figure) Push the mounted wedge into the space between picture tube and the yoke to fix the yoke temporarily.
4. Put other wedge into bottom space and remove the cover paper to stick.
5. Tilt front of the yoke right or left to obtain better convergence in circumference. (See figure)
6. Keep the yoke position and put another wedge in either upper space. Remove cover paper and stick the wedge on picture tube to fix the yoke.
7. Detach the temporarily mounted wedge and put it in another upper space. Stick it on picture tube to fix the yoke.
8. After fixing three wedges, recheck overall convergence. Tighten the screw firmly to fix the yoke and check the yoke is firm.
9. Stick 3 adhesive tapes on wedges.

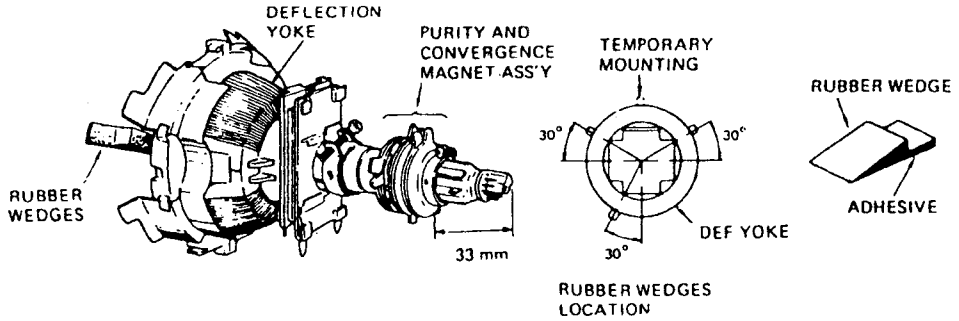
CONVERGENCE COMPENSATOR

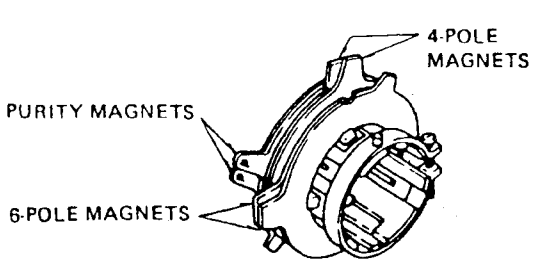
Compensators L462A and L462B are used to correct misconvergence (Red-Green) at the top center or bottom center on screen, when the misconvergence is still evident even though the yoke adjustment is tried. Compensator L462C is also used to correct misconvergence (Vertical shift of Red or Blue) at four corners on screen.

1. To correct horizontal misconvergence (Red-Green), put compensator L462A on the yoke back (see figure right) to find a position for minimizing misconvergence. Mark the position and remove protective paper on the rear of L462A to stick it in place. Apply adhesives on buth yoke and L462A.
2. To correct vertical misconvergence (Red-Green), put the tips of compensator L462B into either of the holes on the yoke core and apply adhesives.
3. To correct up or down shift of Red at top right or bottom right corner, put compensator L462C at point 1 ve 2 or the pisture tube (see figure right.) to find a position for minimizing misconvergence. Mark the position and remove protective paper on the rear of L462C to stick it in place.

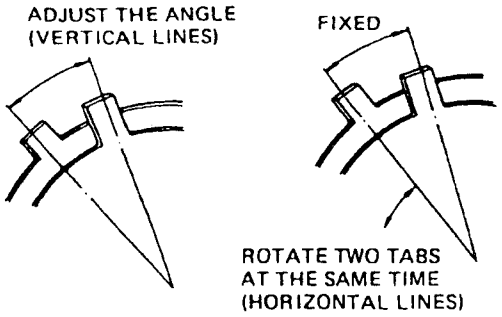




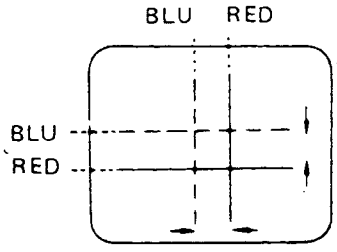




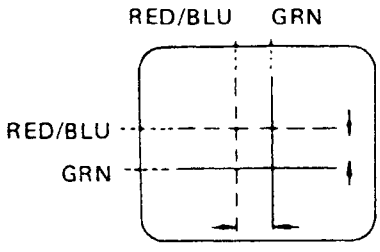
CONVERGENCE MAGNET ASSEMBLY



ADJUSTMENT OF MAGNETS

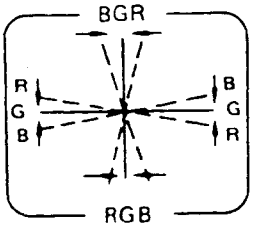


4-POLE MAGNETS MOVEMENT

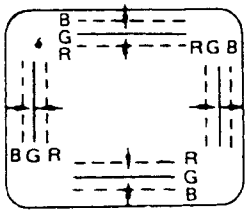


6-POLE MAGNETS MOVEMENT

Centre Convergence by Convergence Magnets



INCLINE THE YOKE UP (OR DOWN)



INCLINE THE YOKE RIGHT (OR LEFT)

Circumference Convergence by DEF Yoke

Dot Movement Pattern