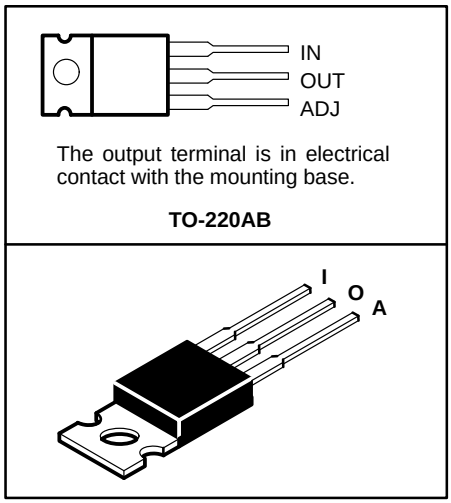
TL783C, TL783Y
HIGH-VOLTAGE ADJUSTABLE REGULATOR

SLVS036C – SEPTEMBER 1981 – REVISED APRIL 1997

- **Output Adjustable From 1.25 V to 125 V When Used With an External Resistor Divider**
- **700-mA Output Current**
- **Full Short-Circuit, Safe-Operating-Area, and Thermal Shutdown Protection**
- **0.001%/V Typical Input Voltage Regulation**
- **0.15% Typical Output Voltage Regulation**
- **76-dB Typical Ripple Rejection**
- **Standard TO-220AB Package**

KC PACKAGE
(TOP VIEW)



description

The TL783C is an adjustable three-terminal high-voltage regulator with an output range of 1.25 V to 125 V and a DMOS output transistor capable of sourcing more than 700 mA. It is designed for use in high-voltage applications where standard bipolar regulators cannot be used. Excellent performance specifications, superior to those of most bipolar regulators, are achieved through circuit design and advanced layout techniques.

As a state-of-the-art regulator, the TL783C combines standard bipolar circuitry with high-voltage double-diffused MOS transistors on one chip to yield a device capable of withstanding voltages far higher than standard bipolar integrated circuits. Because of its lack of secondary breakdown and thermal runaway characteristics usually associated with bipolar outputs, the TL783C maintains full overload protection while operating at up to 125 V from input to output. Other features of the device include current limiting, safe-operating-area (SOA) protection, and thermal shutdown. Even if ADJ is inadvertently disconnected, the protection circuitry remains functional.

Only two external resistors are required to program the output voltage. An input bypass capacitor is necessary only when the regulator is situated far from the input filter. An output capacitor, although not required, improves transient response and protection from instantaneous output short circuits. Excellent ripple rejection can be achieved without a bypass capacitor at the adjustment terminal.

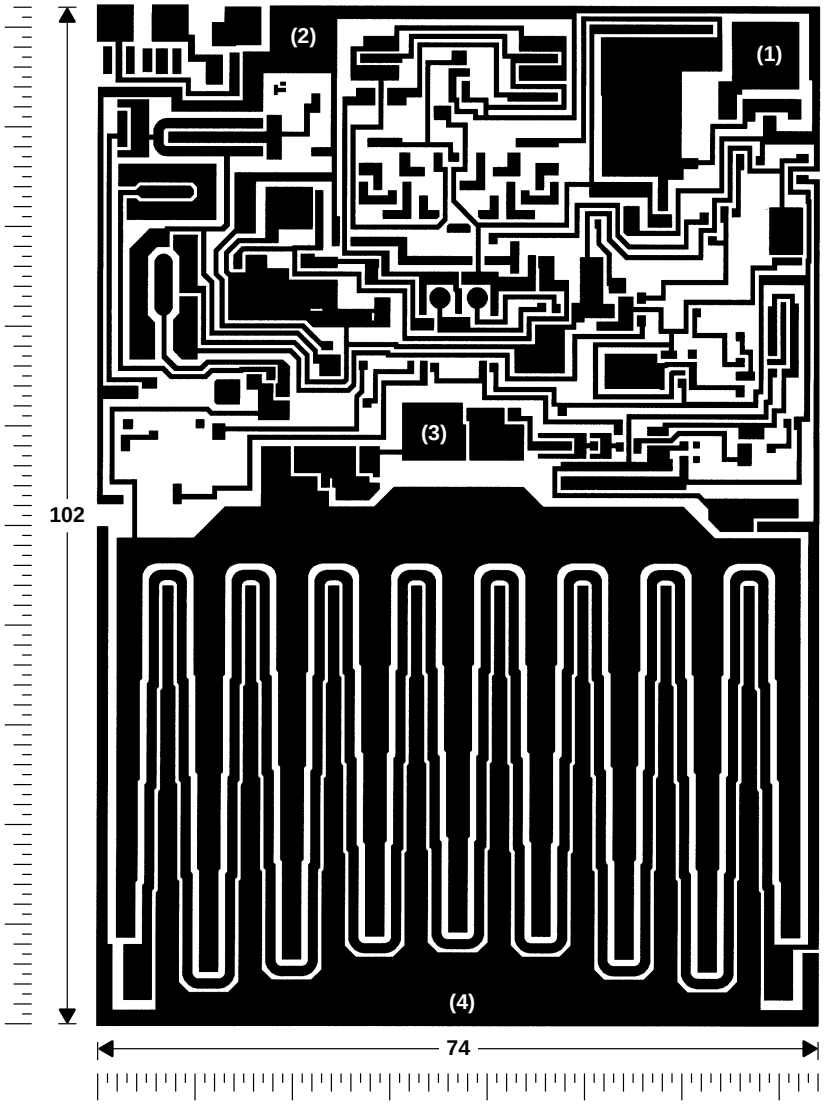
AVAILABLE OPTIONS

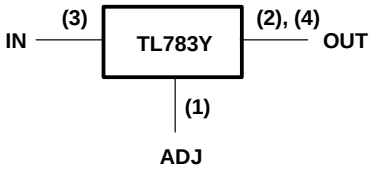
T_J	PACKAGED DEVICE	CHIP FORM (Y)
	HEAT-SINK MOUNTED (3-PIN) (KC)	
0°C to 125°C	TL783CKC	TL783Y

TL783Y chip information

This chip, when properly assembled, displays characteristics similar to those of the TL783C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

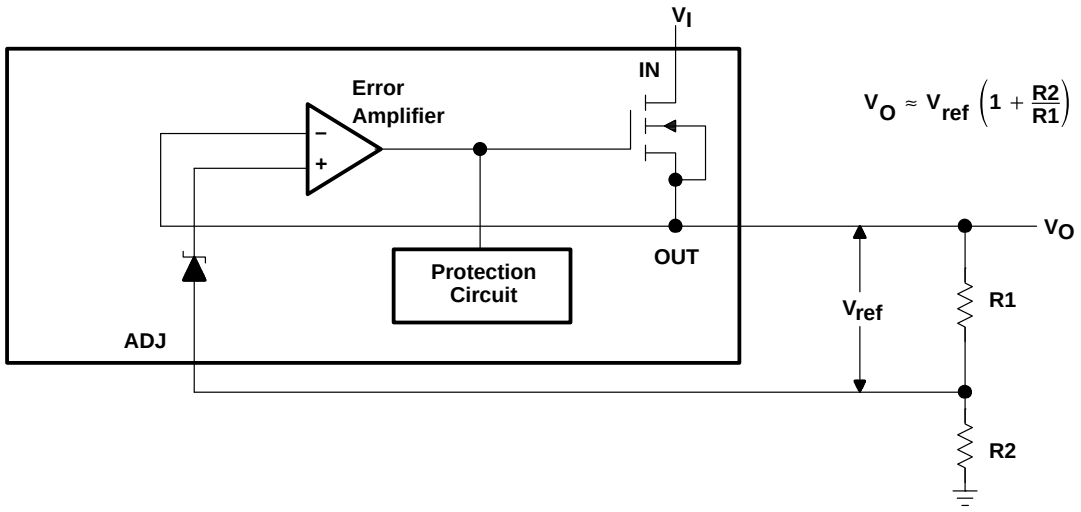
$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

OUTPUT TERMINAL MUST BE BONDED TO BOTH 2 AND 4

functional block diagram



absolute maximum ratings over operating temperature range (unless otherwise noted)†

Input-to-output differential voltage, $V_I - V_O$ . . . . . 125 V
Continuous total power dissipation at (or below) T_A = 25°C (see Note 1) . . . . . 2 W
Continuous total power dissipation at (or below) T_C = 70°C (see Note 1) . . . . . 20 W
Operating free-air, T_A, case, T_C, or virtual junction, T_J, temperature range . . . . . 0°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: For operation above T_A = 25°C or T_C = 70°C, refer to Figures 1 and 2, respectively. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation

FREE-AIR TEMPERATURE DISSIPATION DERATING CURVE

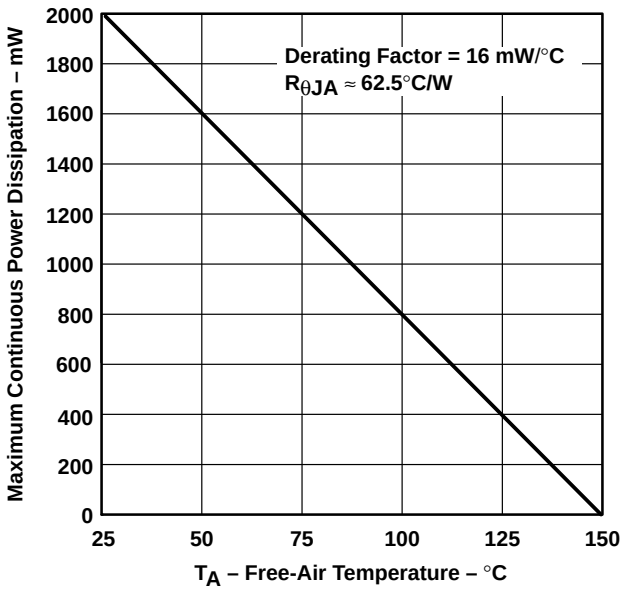


Figure 1

CASE TEMPERATURE DISSIPATION DERATING CURVE

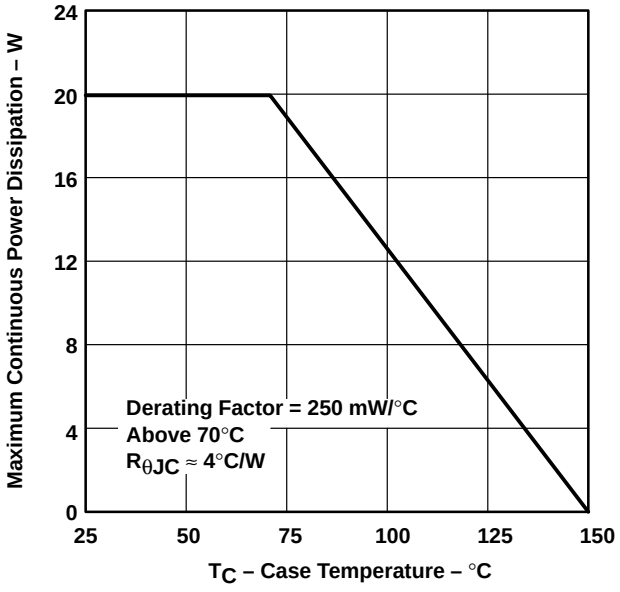


Figure 2

recommended operating conditions

	MIN	MAX	UNIT
Input-to-output voltage differential, $V_I - V_O$		125	V
Output current, I_O	15	700	mA
Operating virtual junction temperature, T_J	0	125	°C

electrical characteristics at $V_I - V_O = 25$ V, $I_O = 0.5$ A, $T_J = 0°C$ to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			TL783C			UNIT
				MIN	TYP	MAX	
Input voltage regulation‡	$V_I - V_O$ = 20 V to 125 V,	P ≤ rated dissipation	T_J = 25°C		0.001	0.01	%/V
			T_J = 0°C to 125°C		0.004	0.02	
Ripple rejection	$\Delta V_{I(PP)}$ = 10 V,	V_O = 10 V,	f = 120 Hz	66	76		dB
Output voltage regulation	I_O = 15 mA to 700 mA,	T_J = 25°C	$V_O \leq$ 5 V		7.5	25	mV
			$V_O \geq$ 5 V		0.15%	0.5%	
	I_O = 15 mA to 700 mA,	P ≤ rated dissipation	$V_O \leq$ 5 V		20	70	mV
			$V_O \geq$ 5 V		0.3%	1.5%	
Output voltage change with temperature					0.4%		
Output voltage long-term drift	1000 hours at T_J = 125°C,	$V_I - V_O$ = 125 V,	See Note 2		0.2%		
Output noise voltage	f = 10 Hz to 10 kHz,	T_J = 25°C			0.003%		
Minimum output current to maintain regulation	$V_I - V_O$ = 125 V					15	mA
Peak output current	$V_I - V_O$ = 25 V,	t = 1 ms			1100		mA
	$V_I - V_O$ = 15 V,	t = 30 ms			715		
	$V_I - V_O$ = 25 V,	t = 30 ms		700	900		
	$V_I - V_O$ = 125 V,	t = 30 ms		100	250		
Input current at ADJ					83	110	μA
Change in input current at ADJ	$V_I - V_O$ = 15 V to 125 V,	I_O = 15 mA to 700 mA,	P ≤ rated dissipation		0.5	5	μA
Reference voltage (OUT to ADJ)	$V_I - V_O$ = 10 V to 125 V, See Note 3	I_O = 15 mA to 700 mA,	P ≤ rated dissipation,	1.2	1.27	1.3	V

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡ Input voltage regulation is expressed here as the percentage change in output voltage per 1-V change at the input.

NOTES: 2. Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

3. Due to the dropout voltage and output current-limiting characteristics of this device, output current is limited to less than 700 mA at input-to-output voltage differentials of less than 25 V.

electrical characteristics at $V_I - V_O = 25$ V, $I_O = 0.5$ A, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TL783Y			UNIT
			MIN	TYP	MAX	
Input voltage regulation‡	$V_I - V_O$ = 20 V to 125 V, P ≤ rated dissipation			0.001		%/V
Ripple rejection	$\Delta V_{I(PP)}$ = 10 V, V_O = 10 V, f = 120 Hz			76		dB
Output voltage regulation	I_O = 15 mA to 700 mA	$V_O \leq$ 5 V		7.5		mV
		$V_O \geq$ 5 V		0.15%		
	I_O = 15 mA to 700 mA, P ≤ rated dissipation	$V_O \leq$ 5 V		20		mV
		$V_O \geq$ 5 V		0.3%		
Output voltage change with temperature				0.4%		
Output noise voltage	f = 10 Hz to 10 kHz			0.003%		
Peak output current	$V_I - V_O$ = 25 V, t = 1 ms			1100		mA
	$V_I - V_O$ = 15 V, t = 30 ms			715		
	$V_I - V_O$ = 25 V, t = 30 ms			900		
	$V_I - V_O$ = 125 V, t = 30 ms			250		
Adjustment-terminal current				83		µA
Change in adjustment-terminal current	$V_I - V_O$ = 15 V to 125 V, I_O = 15 mA to 700 mA, P ≤ rated dissipation			0.5		µA
Reference voltage (OUT to ADJ)	$V_I - V_O$ = 10 V to 125 V, I_O = 15 mA to 700 mA, P ≤ rated dissipation, See Note 3			1.27		V

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡ Input voltage regulation is expressed here as the percentage change in output voltage per 1-V change at the input.

NOTES: 2 Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

3 Due to the dropout voltage and output current-limiting characteristics of this device, output current is limited to less than 700 mA at input-to-output voltage differentials of less than 25 V.

TYPICAL CHARACTERISTICS

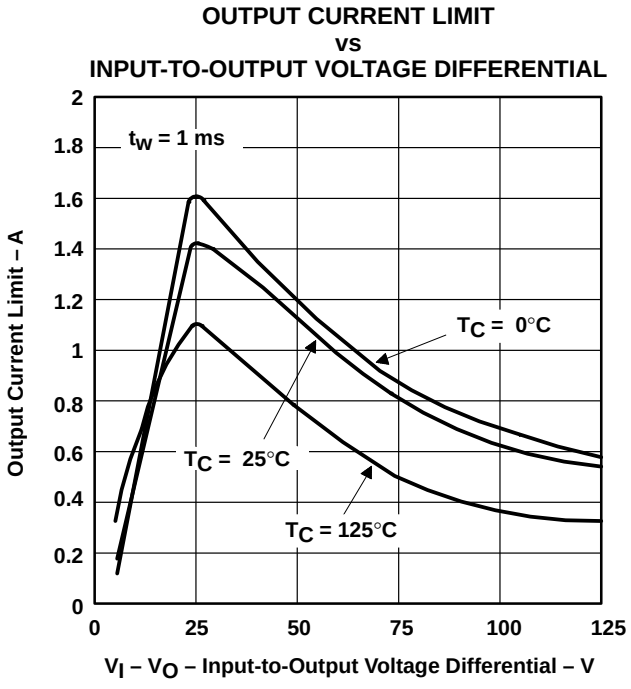


Figure 3

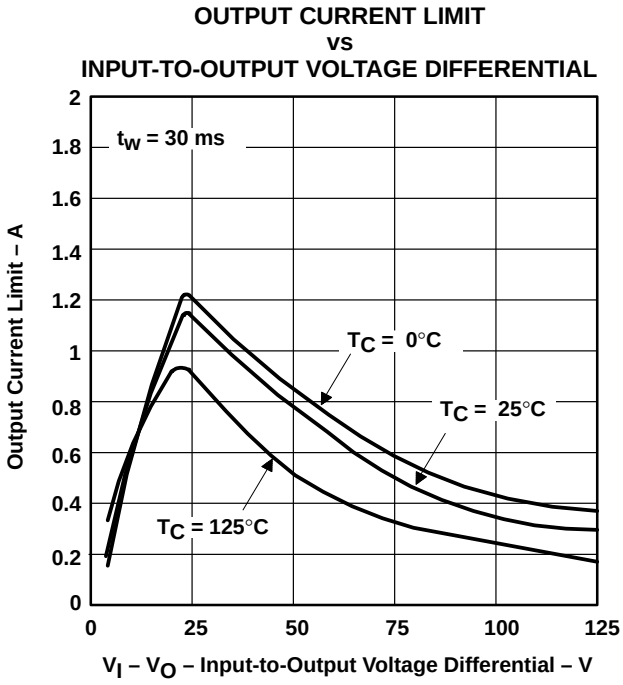


Figure 4

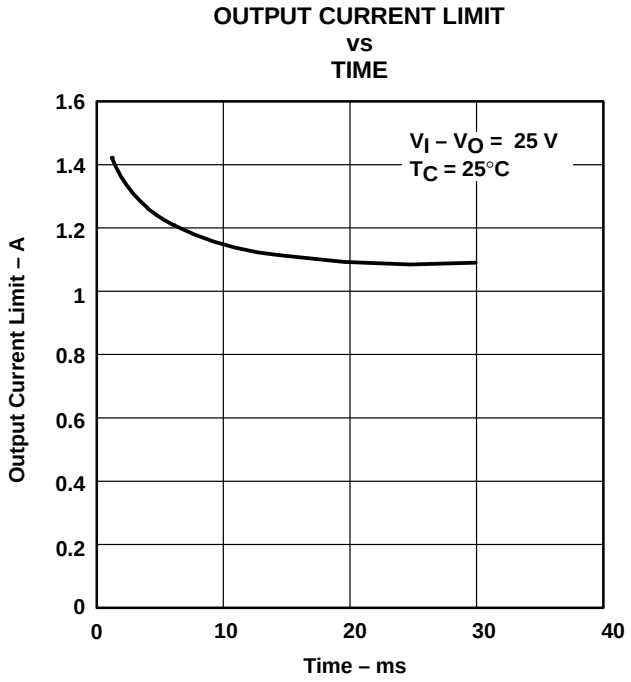


Figure 5

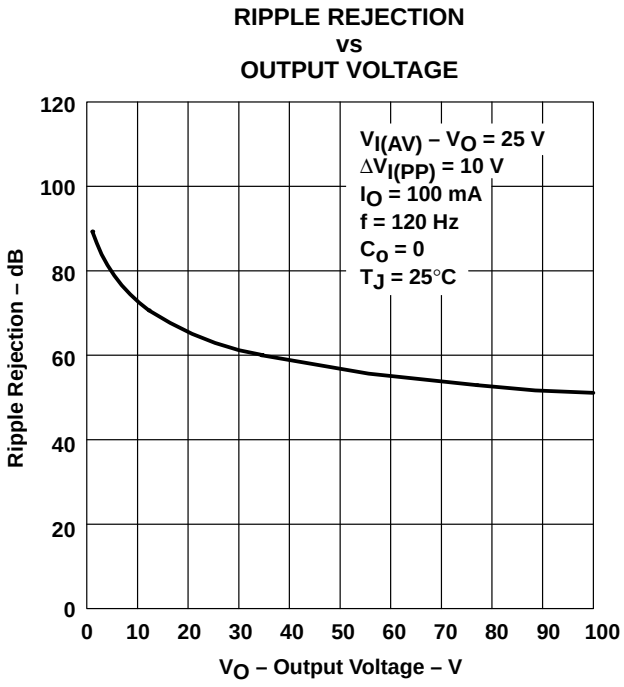


Figure 6

TYPICAL CHARACTERISTICS

RIPPLE REJECTION vs OUTPUT CURRENT

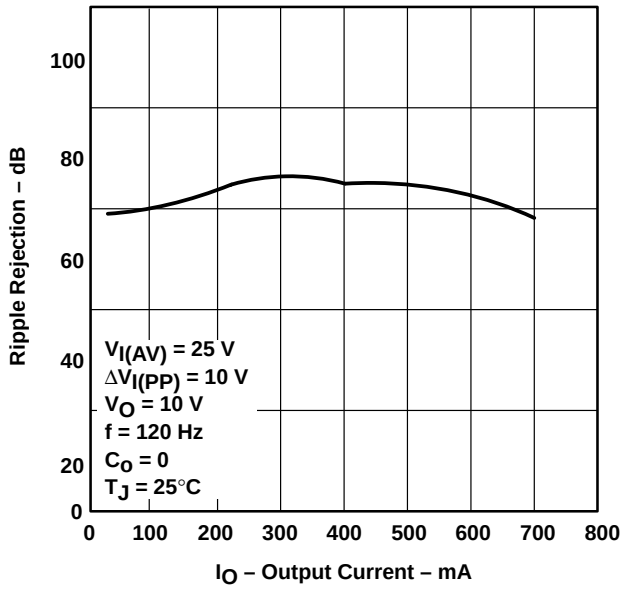


Figure 7

RIPPLE REJECTION vs FREQUENCY

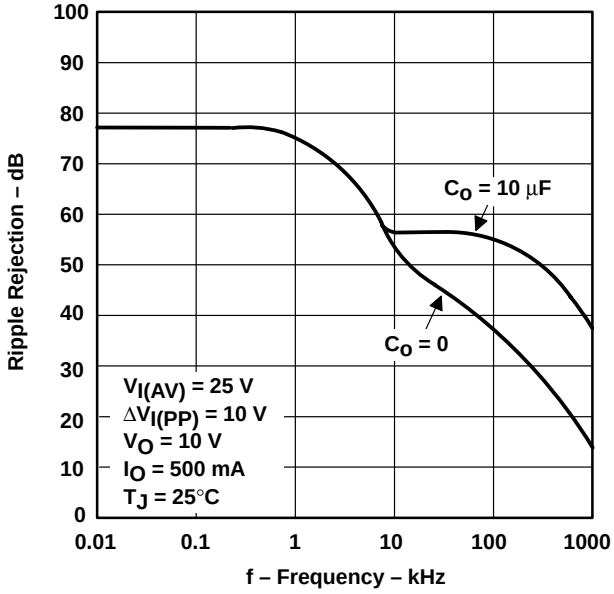


Figure 8

OUTPUT IMPEDANCE vs FREQUENCY

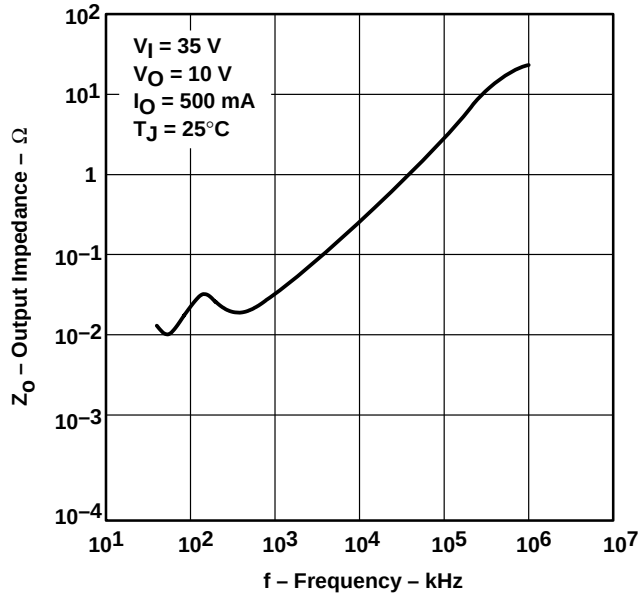


Figure 9

REFERENCE VOLTAGE vs VIRTUAL JUNCTION TEMPERATURE

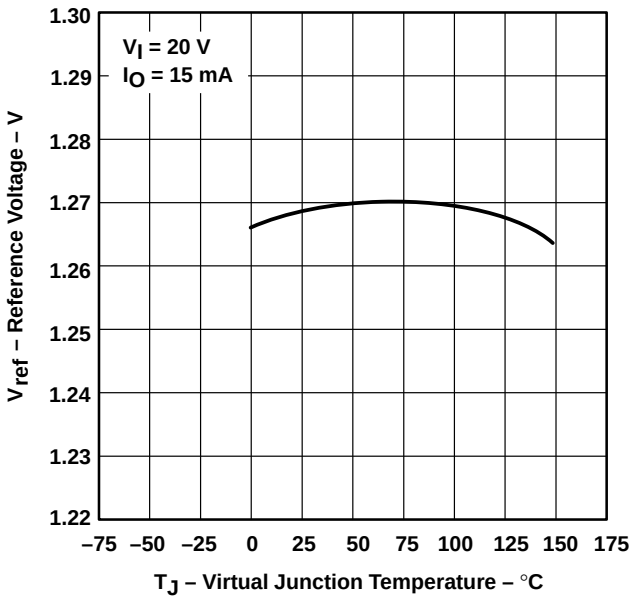


Figure 10

TYPICAL CHARACTERISTICS

INPUT CURRENT AT ADJ vs VIRTUAL JUNCTION TEMPERATURE

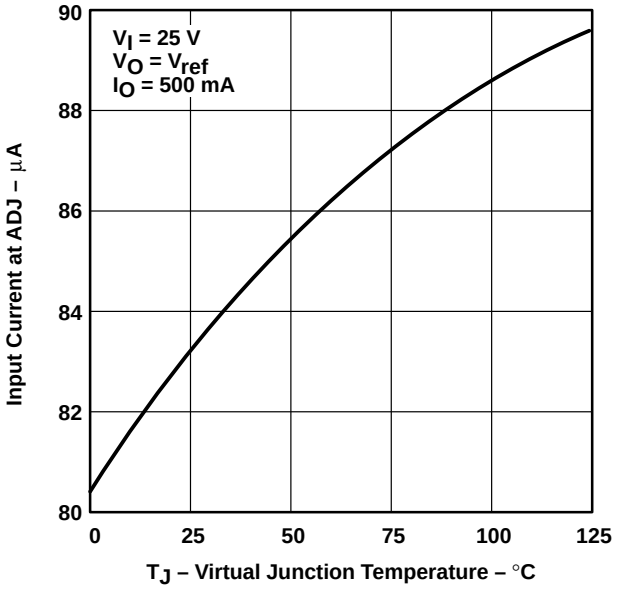


Figure 11

DROPOUT VOLTAGE vs VIRTUAL JUNCTION TEMPERATURE

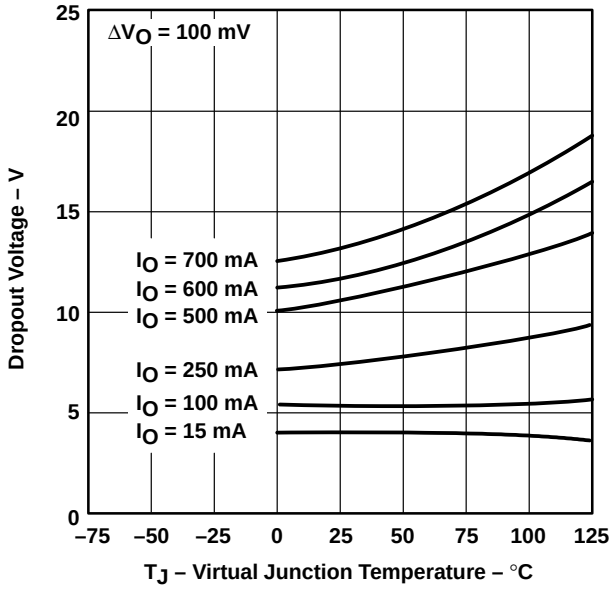


Figure 12

OUTPUT VOLTAGE DEVIATION vs VIRTUAL JUNCTION TEMPERATURE

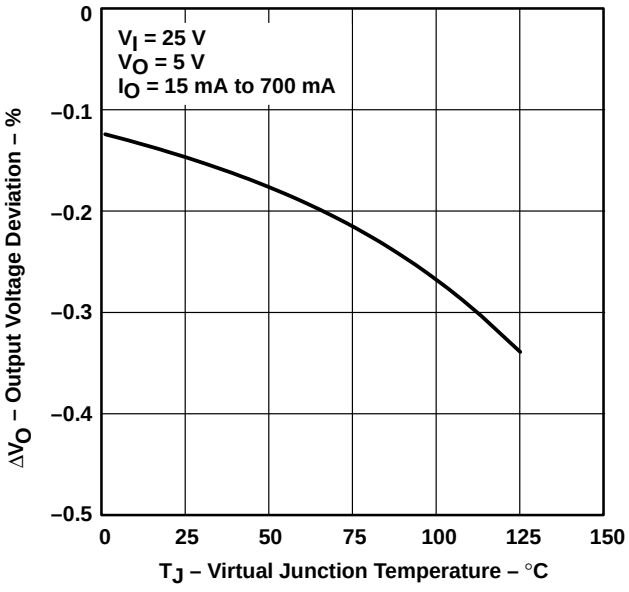
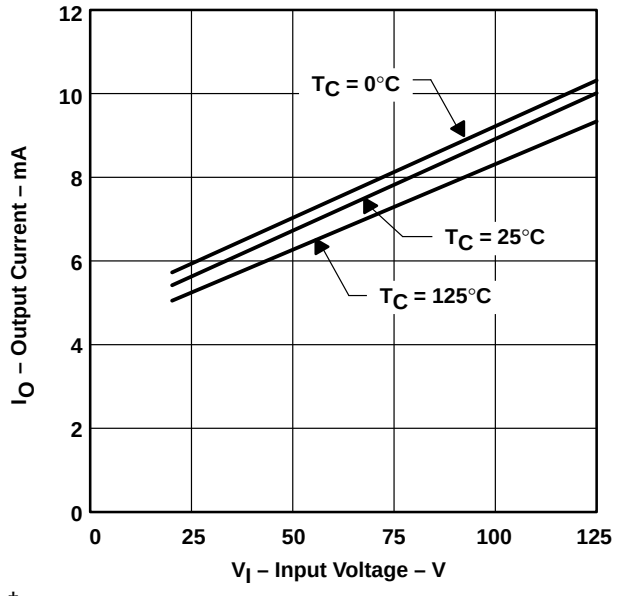


Figure 13

OUTPUT CURRENT† vs INPUT VOLTAGE



† This is the minimum current required to maintain voltage regulation.

Figure 14

TYPICAL CHARACTERISTICS

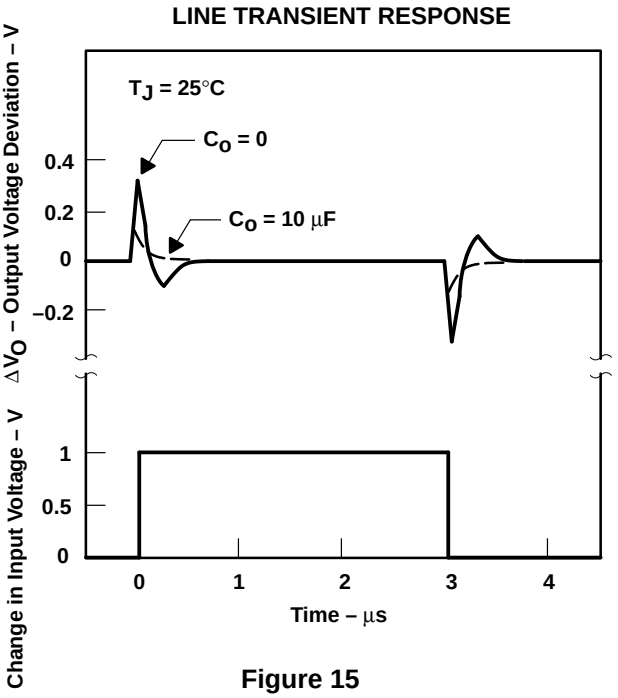


Figure 15

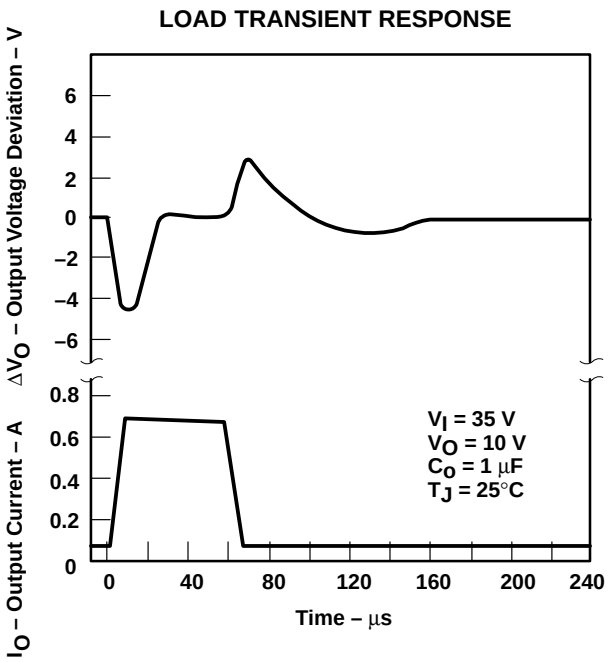


Figure 16

DESIGN CONSIDERATIONS

The internal reference (see functional block diagram) generates 1.25 V nominal (V_{ref}) between OUT and ADJ. This voltage is developed across R1 and causes a constant current to flow through R1 and the programming resistor R2, giving an output voltage of:

$$V_O = V_{ref} (1 + R2/R1) + I_{I(ADJ)} (R2)$$

or

$$V_O \sim V_{ref} (1 + R2/R1).$$

The TL783C was designed to minimize the input current at ADJ and maintain consistency over line and load variations, thereby minimizing the associated (R2) error term.

To maintain $I_{I(ADJ)}$ at a low level, all quiescent operating current is returned to the output terminal. This quiescent current must be sunk by the external load and is the minimum load current necessary to prevent the output from rising. The recommended R1 value of 82 Ω provides a minimum load current of 15 mA. Larger values can be used when the input-to-output differential voltage is less than 125 V (see output current curve, Figure 14) or when the load sinks some portion of the minimum current.

bypass capacitors

The TL783C regulator is stable without bypass capacitors; however, any regulator becomes unstable with certain values of output capacitance if an input capacitor is not used. Therefore, the use of input bypassing is recommended whenever the regulator is located more than four inches from the power-supply filter capacitor. A 1-μF tantalum or aluminum electrolytic capacitor is usually sufficient.

DESIGN CONSIDERATIONS

bypass capacitors (continued)

Adjustment-terminal capacitors are not recommended for use on the TL783C because they can seriously degrade load transient response as well as create a need for extra protection circuitry. Excellent ripple rejection is presently achieved without this added capacitor.

Due to the relatively low gain of the MOS output stage, output voltage dropout may occur under large load transient conditions. The addition of an output bypass capacitor greatly enhances load transient response as well as prevents dropout. For most applications, it is recommended that an output bypass capacitor be used with a minimum value of:

$$C_O\ (\mu F) = 15/V_O$$

Larger values provide proportionally better transient response characteristics.

protection circuitry

The TL783C regulator includes built-in protection circuits capable of guarding the device against most overload conditions encountered in normal operation. These protective features are current limiting, safe-operating-area protection, and thermal shutdown. These circuits protect the device under occasional fault conditions only. Continuous operation in the current limit or thermal shutdown mode is not recommended.

The internal protection circuits of the TL783C protect the device up to maximum-rated V_I as long as certain precautions are taken. If V_I is instantaneously switched on, transients exceeding maximum input ratings may occur, which can destroy the regulator. These are usually caused by lead inductance and bypass capacitors causing a ringing voltage on the input. In addition, when rise times in excess of 10 V/ns are applied to the input, a parasitic npn transistor in parallel with the DMOS output can be turned on causing the device to fail. If the device is operated over 50 V and the input is switched on rather than ramped on, a low-Q capacitor, such as tantalum or aluminum electrolytic should be used rather than ceramic, paper, or plastic bypass capacitors. A Q factor of 0.015 or greater usually provides adequate damping to suppress ringing. Normally, no problems occur if the input voltage is allowed to ramp upward through the action of an ac line rectifier and filter network.

Similarly, when an instantaneous short circuit is applied to the output, both ringing and excessive fall times can result. A tantalum or aluminum electrolytic bypass capacitor is recommended to eliminate this problem. However, if a large output capacitor is used and the input is shorted, addition of a protection diode may be necessary to prevent capacitor discharge through the regulator. The amount of discharge current delivered is dependent on output voltage, size of capacitor, and fall time of V_I. A protective diode (see Figure 17) is required only for capacitance values greater than:

$$C_O\ (\mu F) = 3 \times 10^4/(V_O)^2$$

Care should always be taken to prevent insertion of regulators into a socket with power on. Power should be turned off before removing or inserting regulators.

DESIGN CONSIDERATIONS

protection circuitry (continued)

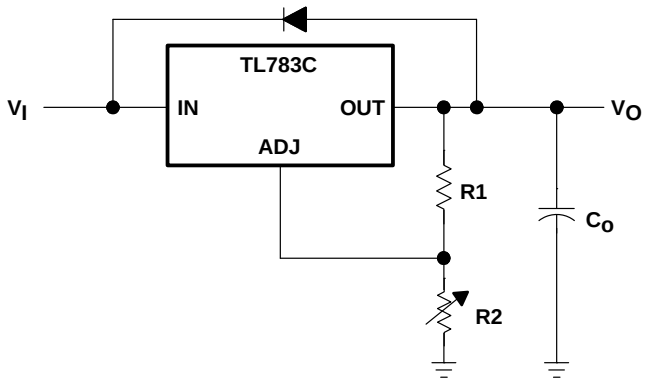


Figure 17. Regulator With Protective Diode

load regulation

The current set resistor (R1) should be located close to the regulator output terminal rather than near the load. This eliminates long line drops from being amplified through the action of R1 and R2 to degrade load regulation. To provide remote ground sensing, R2 should be near the load ground.

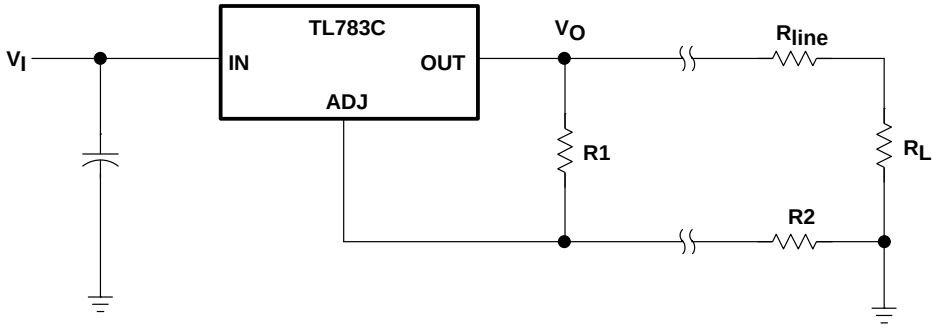
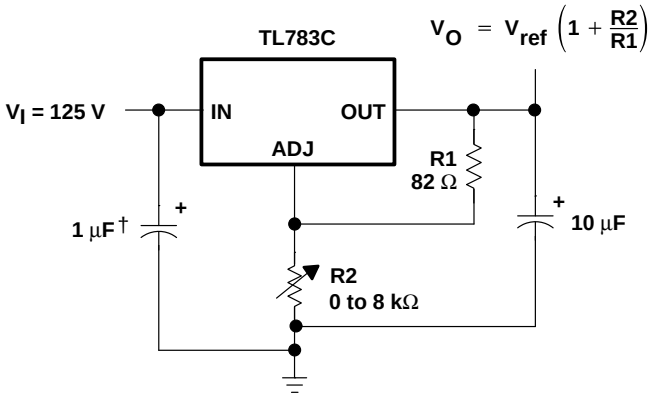


Figure 18. Regulator With Current-Set Resistor

APPLICATION INFORMATION



† Needed if device is more than 4 inches from filter capacitor

Figure 19. 1.25-V to 115-V Adjustable Regulator

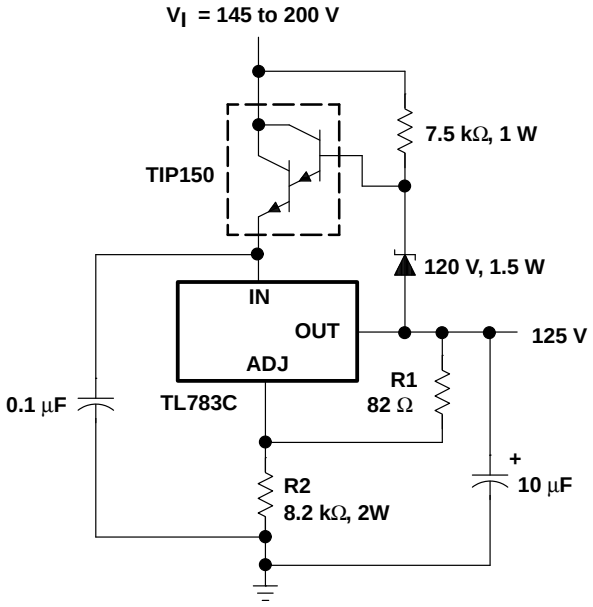


Figure 20. 125-V Short-Circuit-Protected Off-Line Regulator

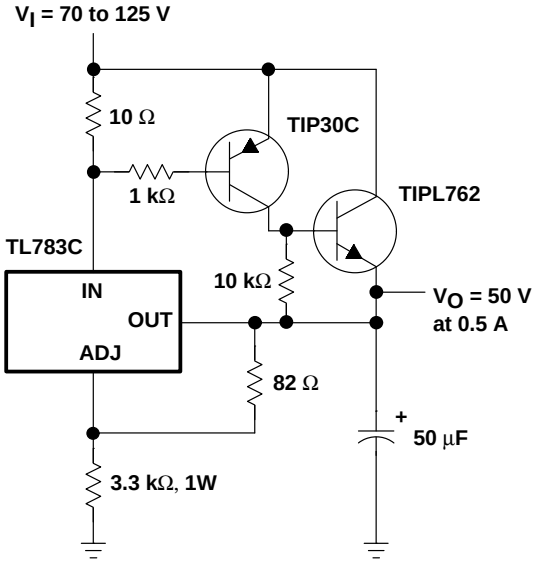


Figure 21. 50-V Regulator With Current Boost

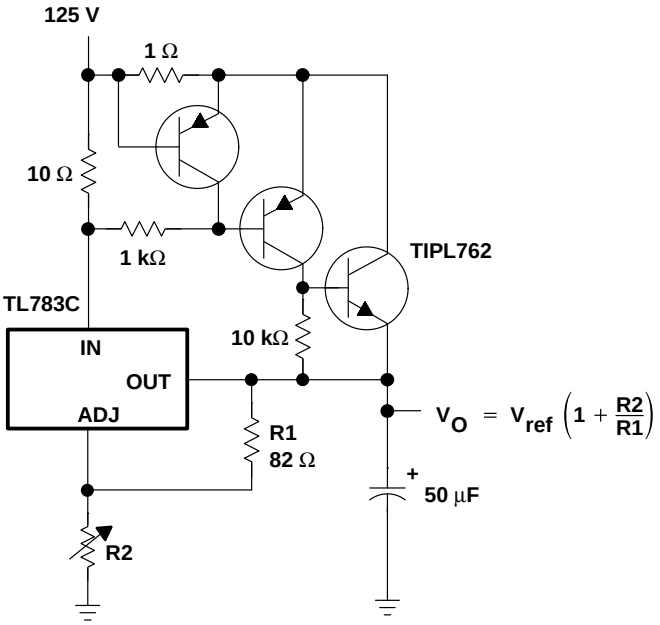


Figure 22. Adjustable Regulator With Current Boost and Current Limit

APPLICATION INFORMATION

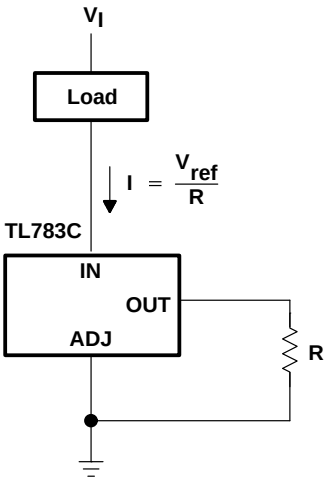


Figure 23. Current-Sinking Regulator

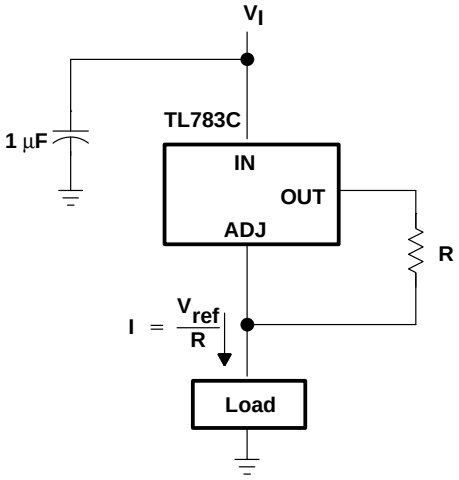


Figure 24. Current-Sourcing Regulator

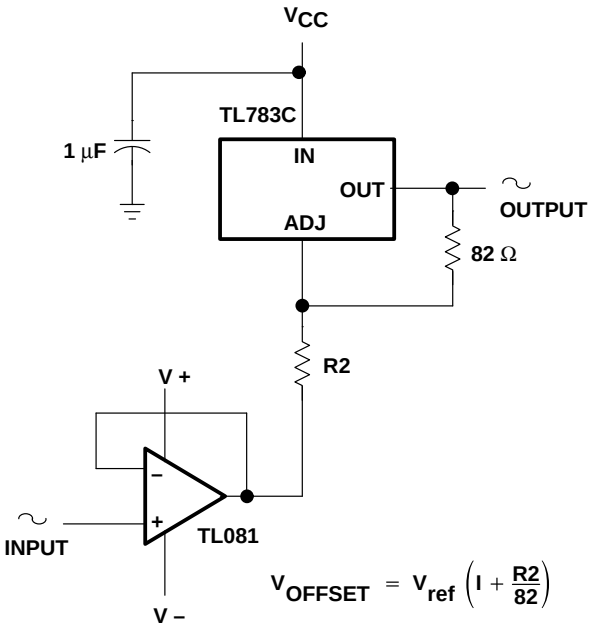


Figure 25. High-Voltage Unity-Gain Offset Amplifier

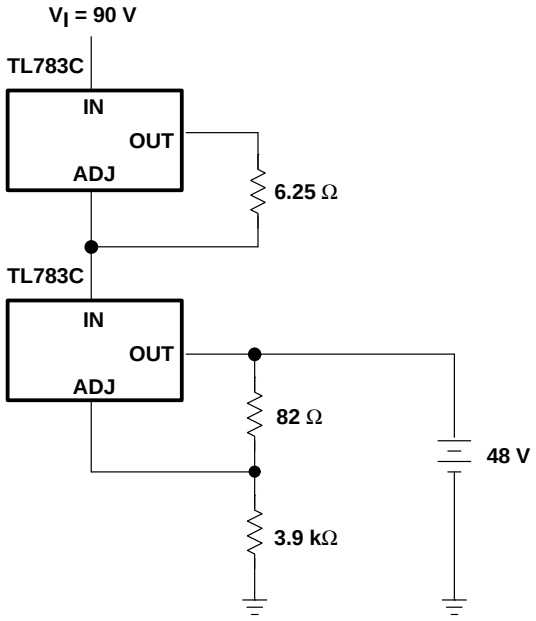
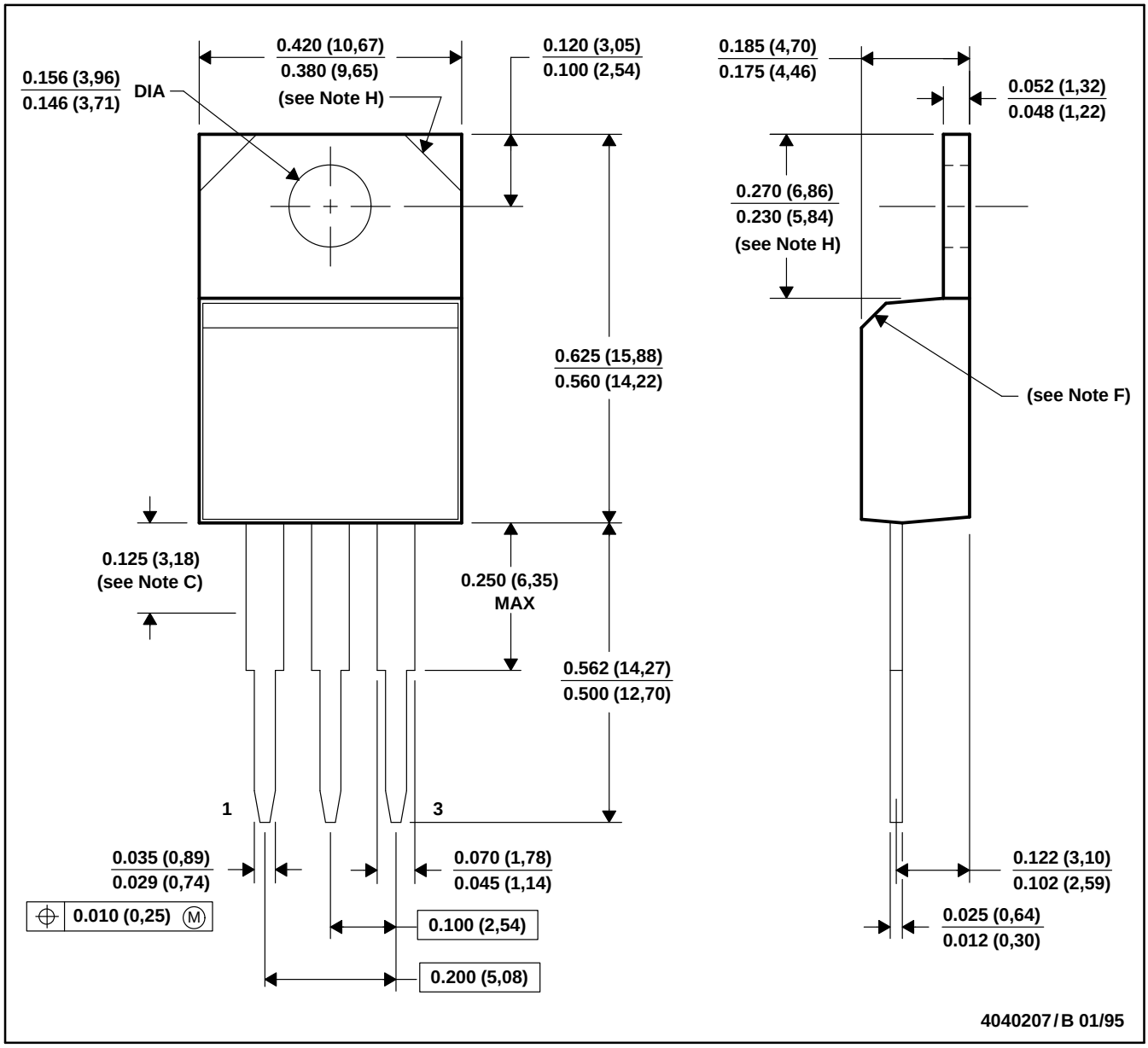


Figure 26. 48-V, 200-mA Float Charger

MECHANICAL DATA

KC (R-PSFM-T3) **PLASTIC FLANGE-MOUNT PACKAGE**



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area.
D. All lead dimensions apply before solder dip.
E. The center lead is in electrical contact with the mounting tab.
F. The chamfer is optional.
G. Falls within JEDEC TO-220AB
H. Tab contour optional within these dimensions