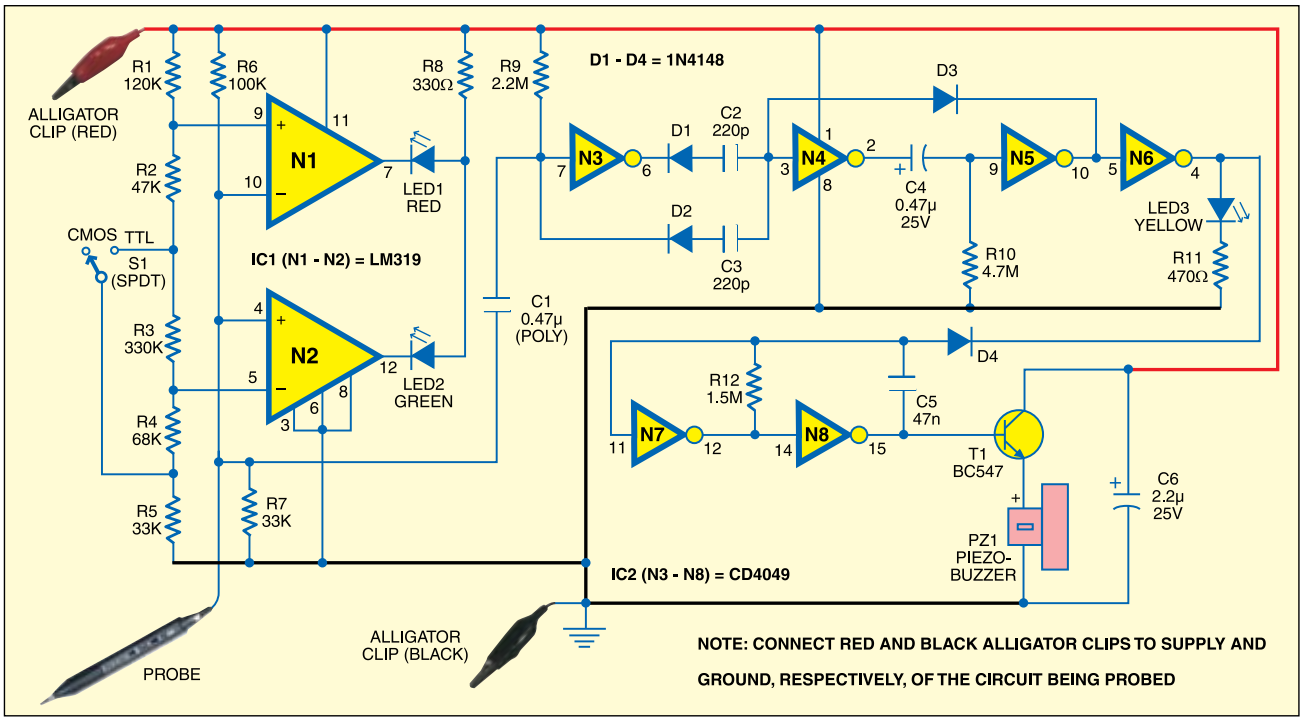
VERSATILE CMOS/TTL LOGIC AND CLOCK PROBE

EFY LAB

For fault diagnosis of any logic circuit, you need a probe that can test the logic level or existence of clock activity. The circuit shown here can be used to test CMOS and TTL logic circuits for logic states and also for the presence of clock activity from a few hertz to more than 10 MHz, at any point of the logic circuit.

Supply for the probe circuit is taken from the circuit under test using alligator clips. In the circuit, LM319 dual-comparator is connected as a window detector. The non-inverting pin of comparator N1 is biased to nearly 2V when switch S1 is in TTL position and 80 per cent of Vcc in CMOS position. The output of N1 goes low only when logic input at the probe tip exceeds the biasing voltage and, as a result, the red LED lights up to indicate logic 1 state at the probe tip.

Similarly, the inverting pin of comparator N2 is biased at nearly 0.8V (in TTL position of switch S1) and 20 per cent of Vcc (in CMOS position of switch S1). Only when the input voltage at probe tip is less than the biasing voltage, will its output drop low to light up the green LED to indicate logic 0 state.



Test Results

Test conditions	Specified level	Observed level	Red LED	Green LED	Yellow LED	Buzzer sound
TTL (5V)						
Low	<0.8V	<0.8V	Off	On	Off	Off
High	>2V	≥2.1V	On	Off	Off	Off
Clock	TTL compatible	1 Hz to 10 MHz or even more	Off	Momentarily on/off	On for 3 seconds	On for 3 seconds
CMOS (12V)						
Low	<2.5V	≤2.35V	Off	On	Off	Off
High	>9.5V	>9.5V	On	Off	Off	Off
Clock	CMOS compatible	1 Hz to 10 MHz or even more	Off	Momentarily on/off	'On' for 3 seconds	'On' for 3 seconds

The probe tip is also connected to the input of CD4049 (N3) via capacitor C1 to pass AC/clock signals. It simply acts as a buffer and couples only the high-to-low going signals at the input/output of the gate to the input of next gate N4.

The output of gate N4 is further coupled to gate N5, which is wired as a monostable. A positive feedback from

the output of gate N5 to the input of gate N4 ensures that unless capacitor C4 (0.47µF) discharges sufficiently via 4.7-mega-ohm resistor, further clock pulses at the input of N4 will have no effect.

Gate N6 is used for driving a yellow LED (indicating oscillatory input at probe tip), which will be switched on for a brief period. The output of gate N6 is further used to inhibit/enable the oscillator formed by gates N7 and N8. It briefly activates the buzzer to beep during mono period, indicating oscillatory input at the probe tip. Thus we have audio-visual indication during clock/oscillatory input at the probe tip. ●